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--MARK--

Schematic Package Supplement to

KANGAROO™

Operation, Maintenance and Service Manual

NOTE

This staple temporarily holds the schematic package together. Remove the staple before using the schematics.



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7L

SP-204 Sheet 1A
3rd printing

Table of Contents

- Sheet 1A You Are Here
- Sheet 1B Upright Kangaroo Game Wiring Diagram (038577-01 A)
- Sheet 2A Ireland-Built Kangaroo Game Wiring Diagram (038451-01 A)
- Sheet 2B Color Raster-Scan Power Supply Wiring Diagram (037669-01 C)
- Sheet 3A Regulator/Audio II PCB Schematic Diagram (035435-06 B)
- Sheet 3B Coin Door Wiring Diagram (037542-01 B), Utility Panel Wiring Diagram (038004-01 B), Fluorescent Light and Speaker Wiring Diagram (035833-01 A)

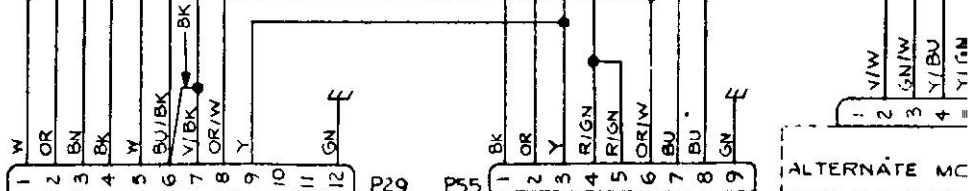
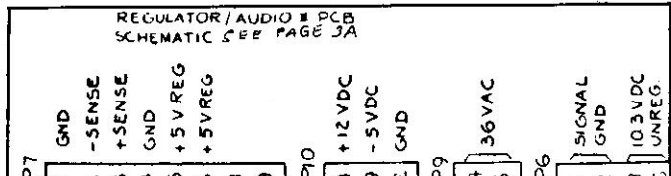
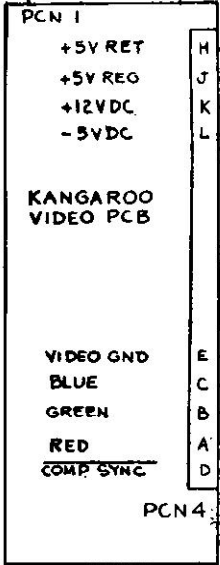
Central Processing Unit (CPU) PCB Schematics (038469-01 A), Sheets 4A-7A

- Sheet 4A Block Diagram
- Sheet 4B Memory Map, CPU Power Input
- Sheet 5A Game Microprocessor, Address Decoder
- Sheet 5B Program ROM, RAM
- Sheet 6A Inputs, Outputs
- Sheet 6B Sound Microprocessor, Address Decoder
- Sheet 7A Custom Microcomputer

Video PCB Schematics (038468-01 A), Sheets 7B-11B

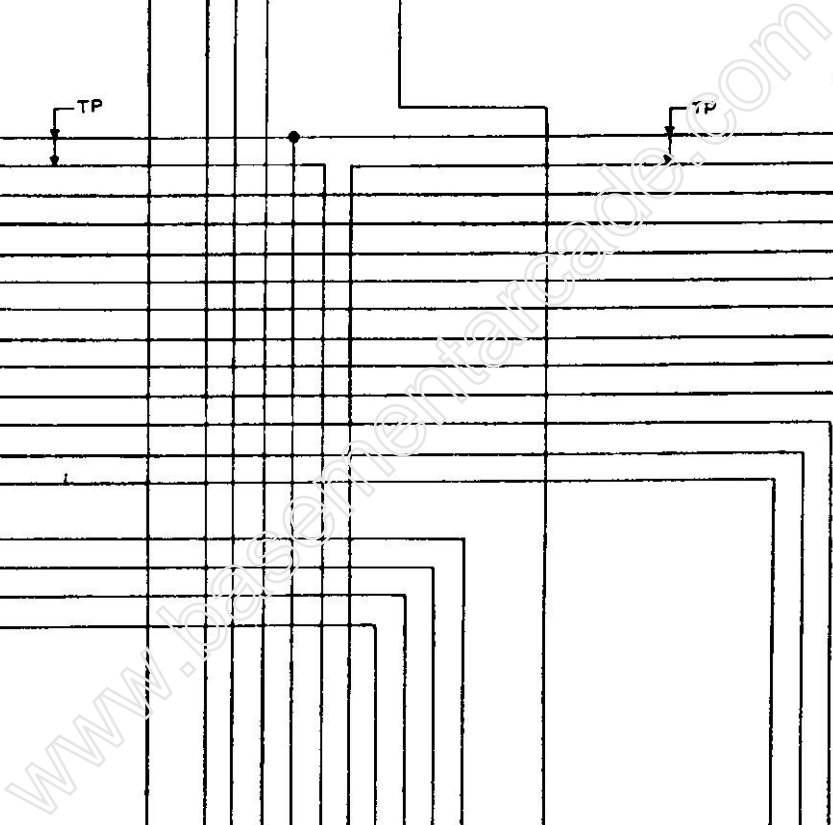
- Sheet 7B Block Diagram
- Sheet 8A Dynamic RAM Timing Diagram, Video Power Input
- Sheet 8B Clock, Sync Chain and Timing Signals, Dynamic RAM Control, Address Decoding
- Sheet 9A DMA Control, Dynamic RAM Video Address and Flip
- Sheet 9B Picture ROM Address Selector, Picture ROM
- Sheet 10A Dynamic RAM Address from CPU and for DMA
- Sheet 10B Dynamic RAM Data Selector, Address Selector, and Control Latches
- Sheet 11A Playfield (Dynamic RAM A)
- Sheet 11B Motion Object (Dynamic RAM B), Video Output
- Sheet 12A Electrohome 19-Inch Color Raster-Scan Video Display Schematic Diagram

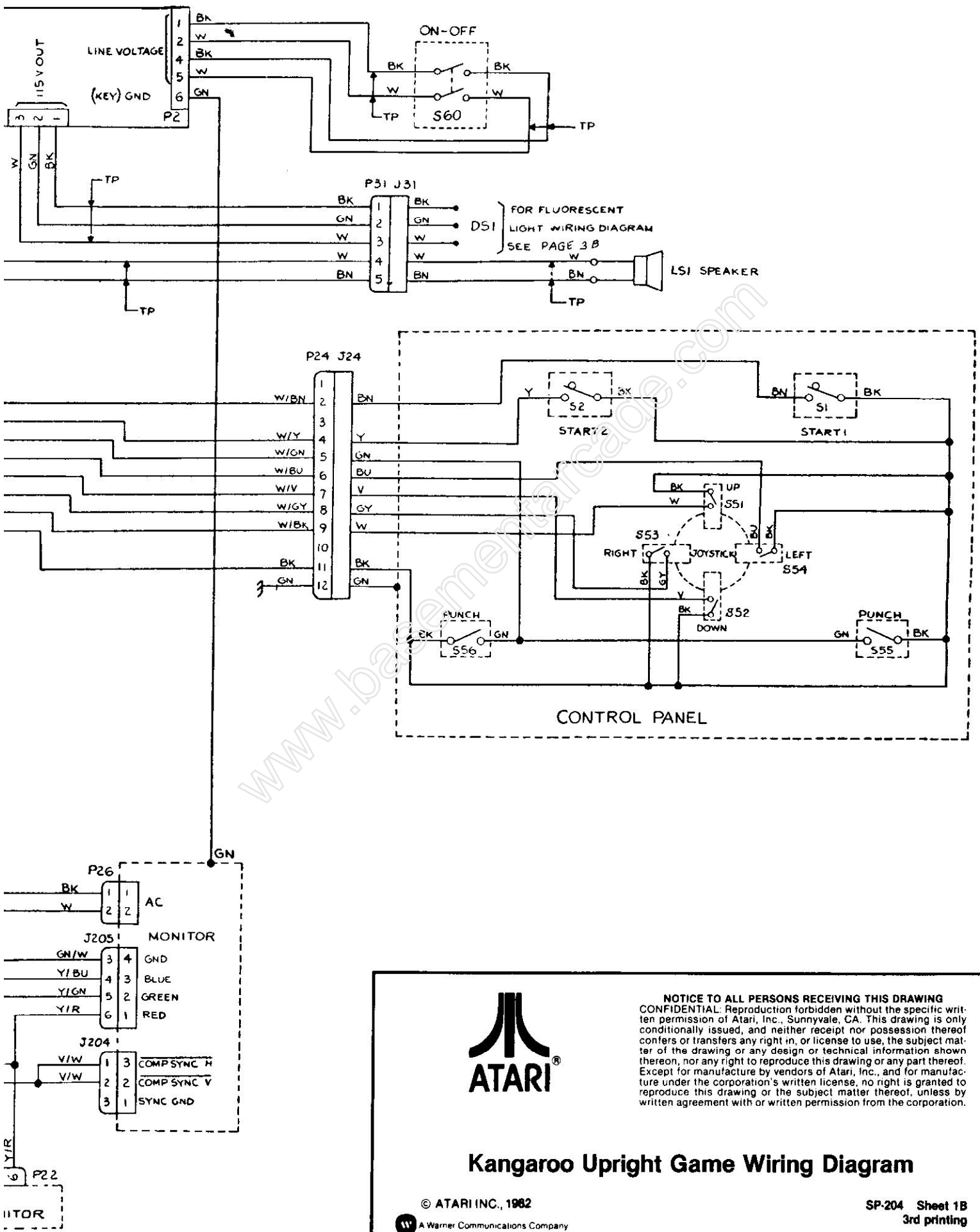
KANGAROO CPU PCB



FOR COMPONENT WIRING
DIAGRAM SEE PAGE 3B

FOR COIN DOOR WIRING
DIAGRAM SEE PAGE 3B





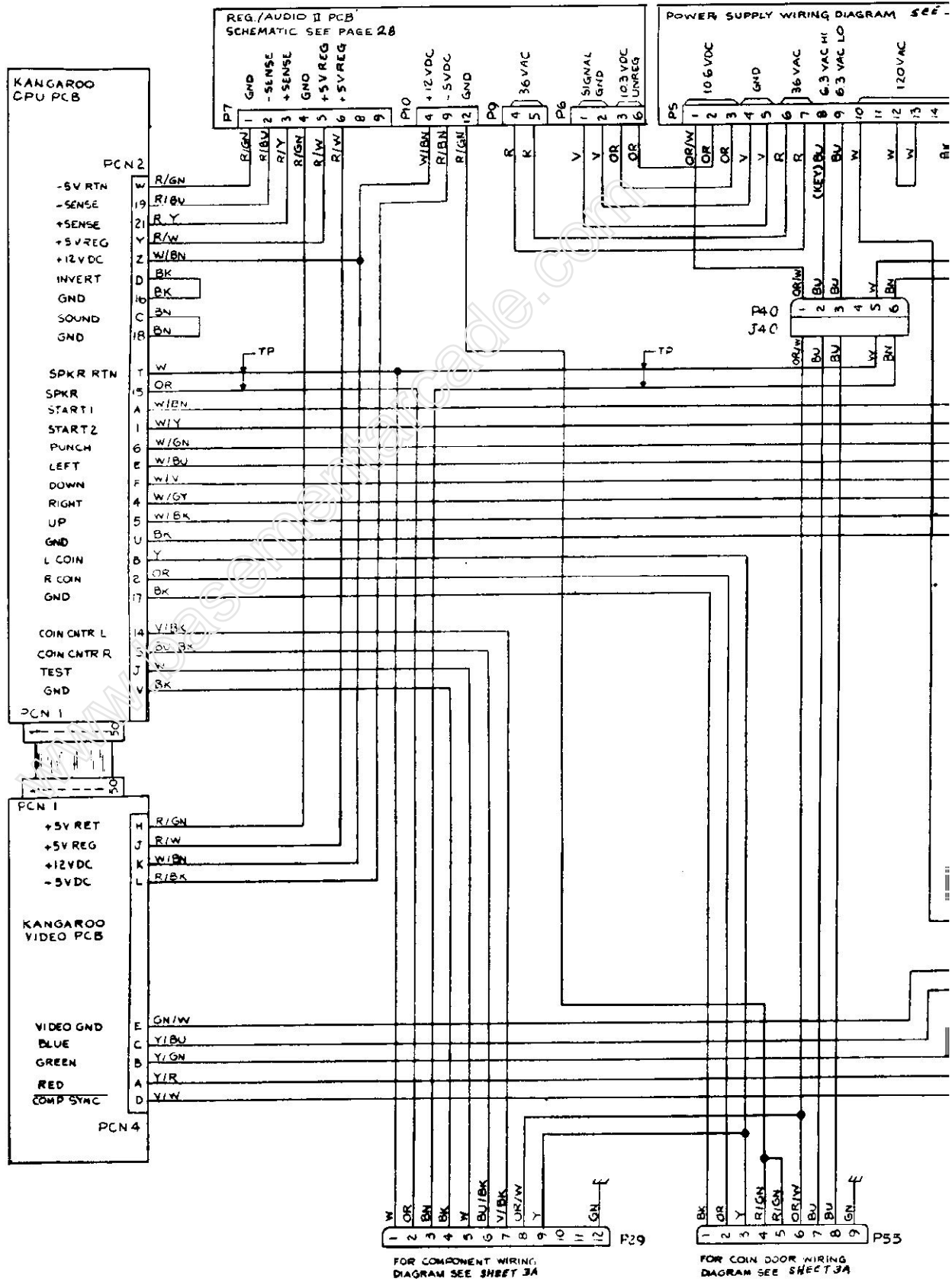
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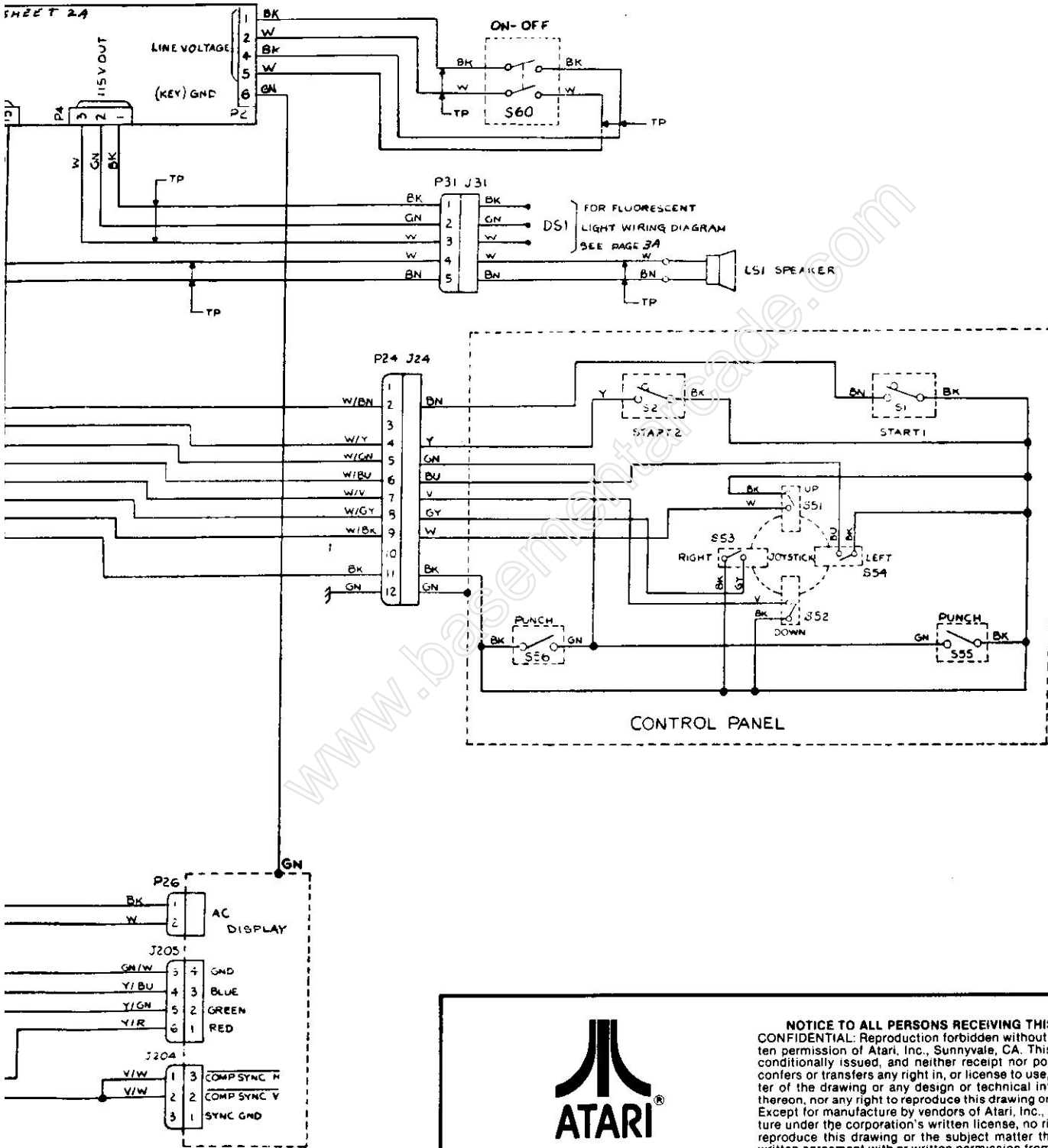
Kangaroo Upright Game Wiring Diagram

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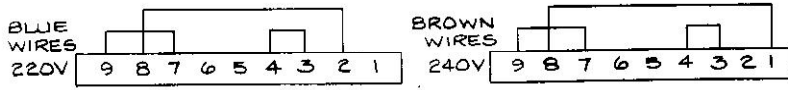
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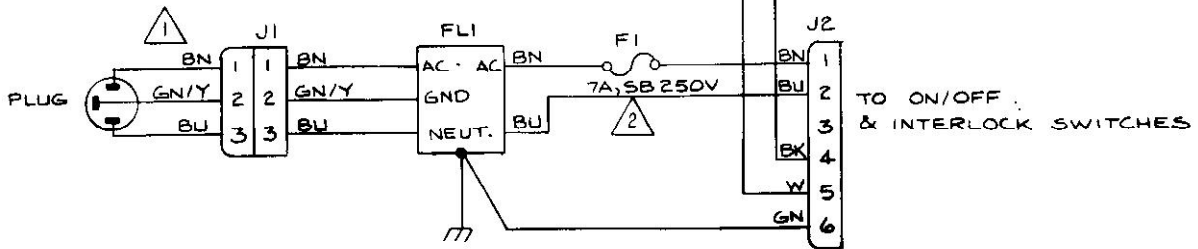
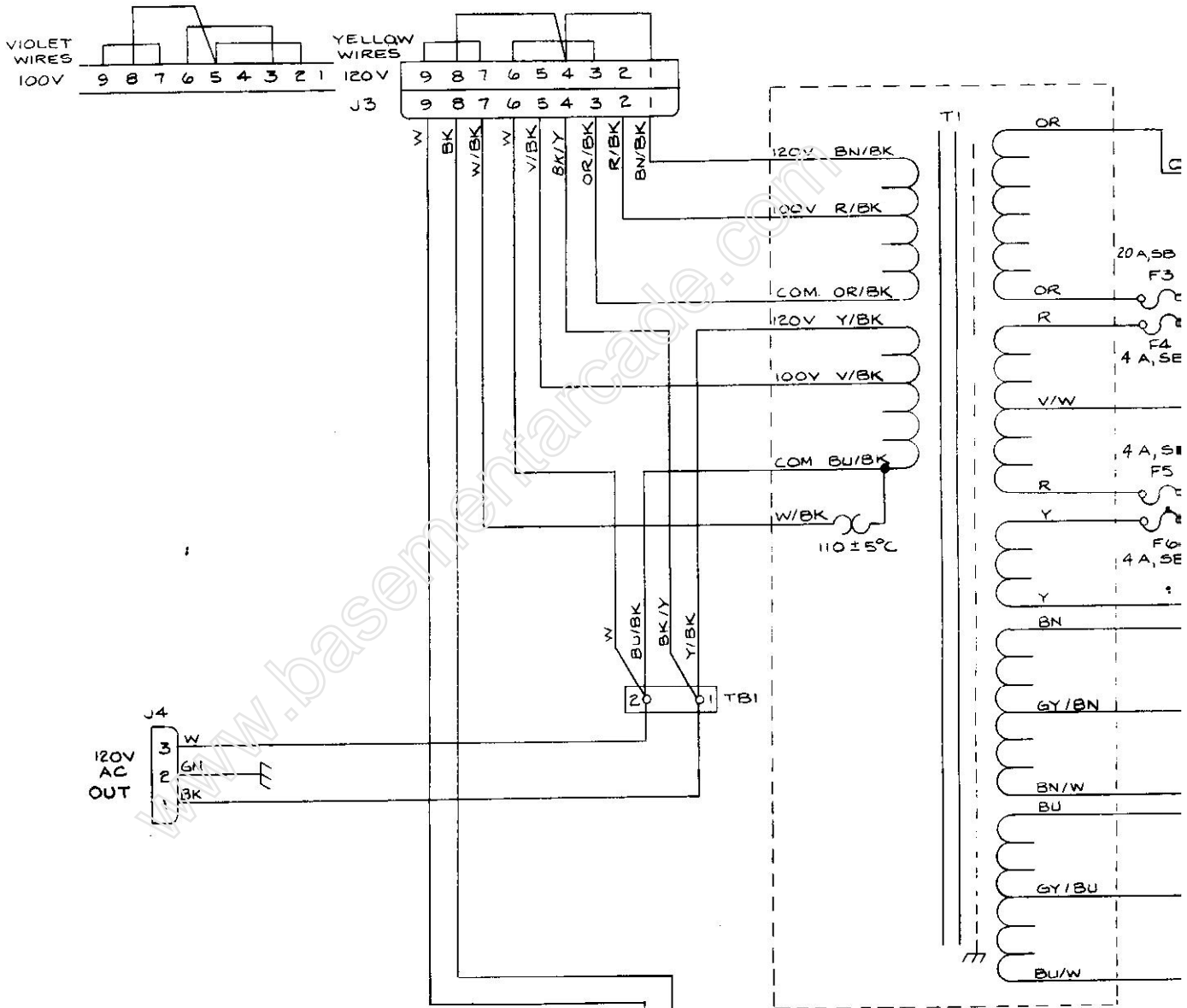


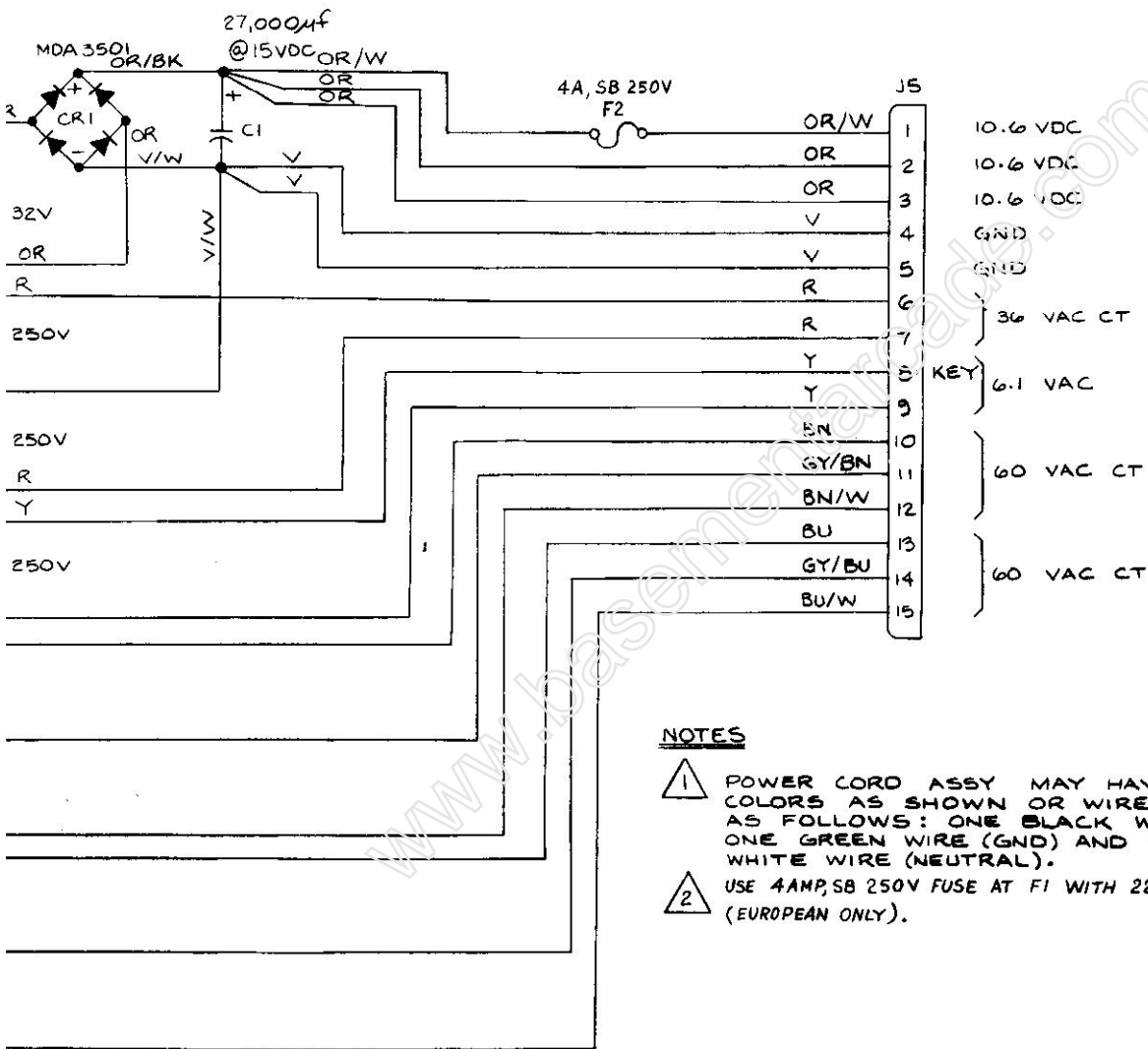
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Ireland-Built Kangaroo Game Wiring Diagram



VOLTAGE SELECTION BLOCKS





NOTES

- 1 POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
- 2 USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).



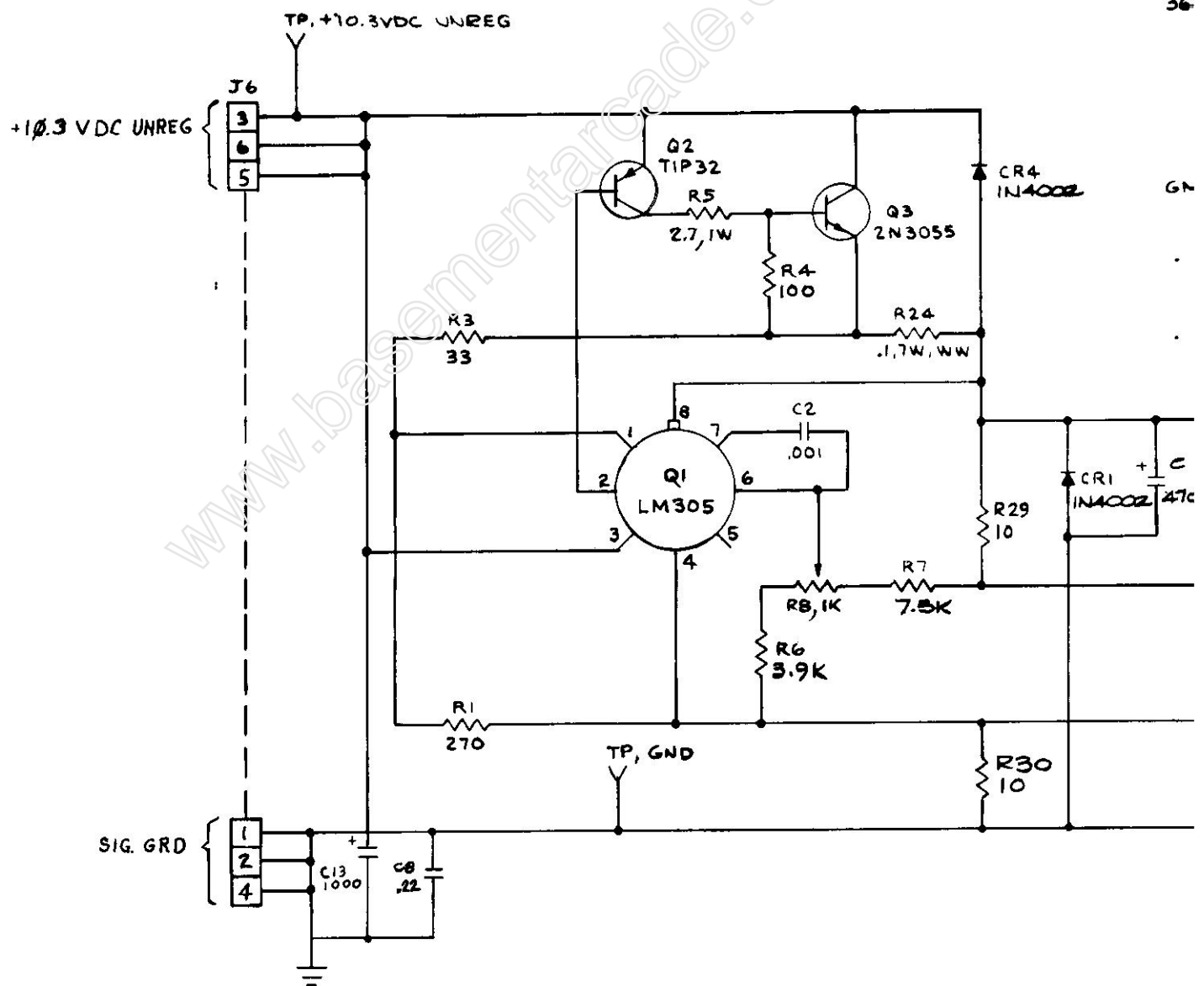
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Kangaroo Power Supply

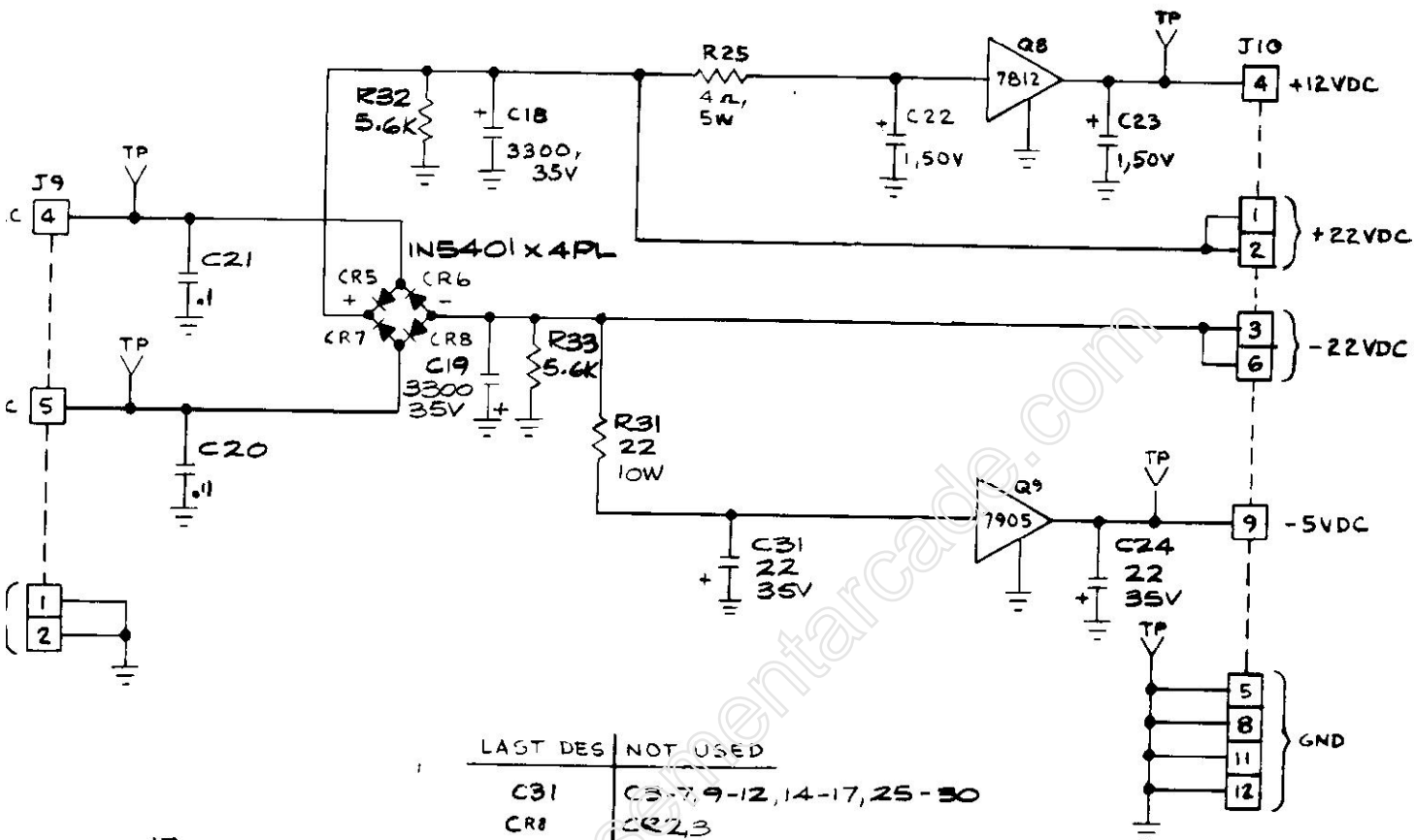
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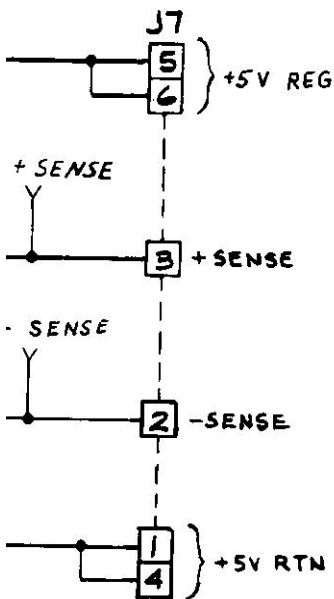
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LAST DES	NOT USED
C31	C3-7, 9-12, 14-17, 25-30
CR8	CR2, 3
Q11	Q10, 11, 4, 6
R33	R2, 9-23, 26-28



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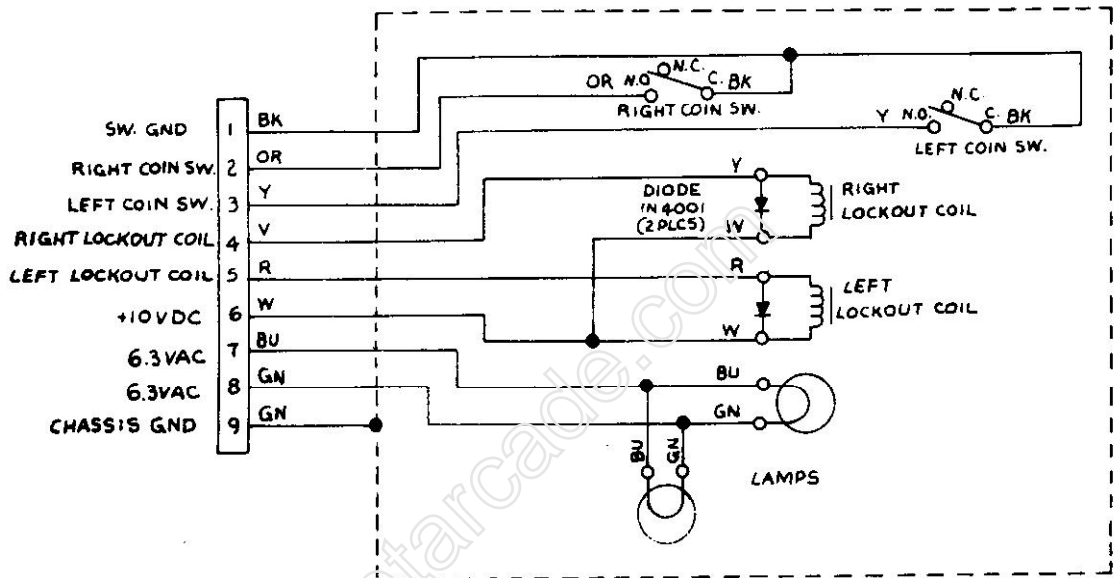
Kangaroo Reg/Audio II PCB Schematic Diagram

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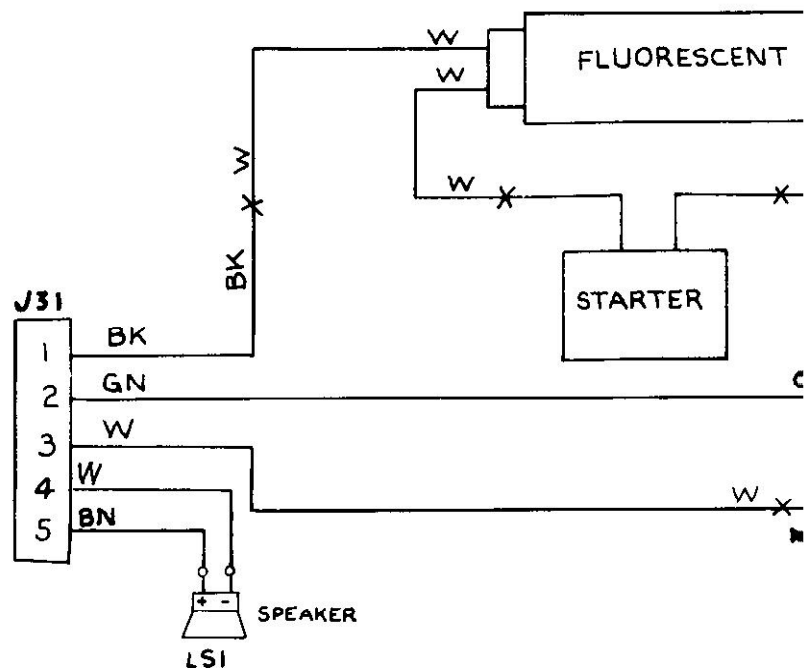
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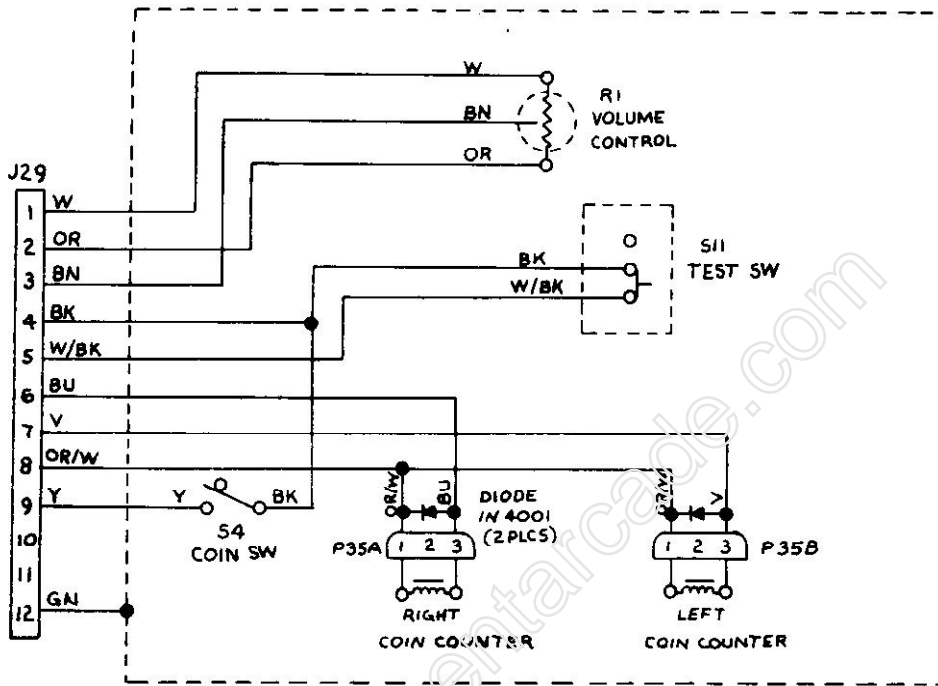
Coin Door Wiring Diagram



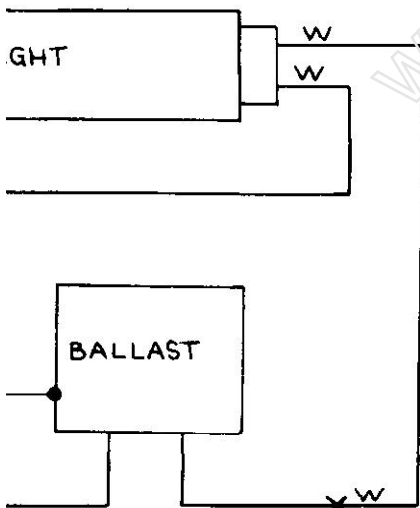
Fluorescent Light and Spea



Utility Panel Wiring Diagram



er Wiring Diagram



— SPLICE (5 PLCS)



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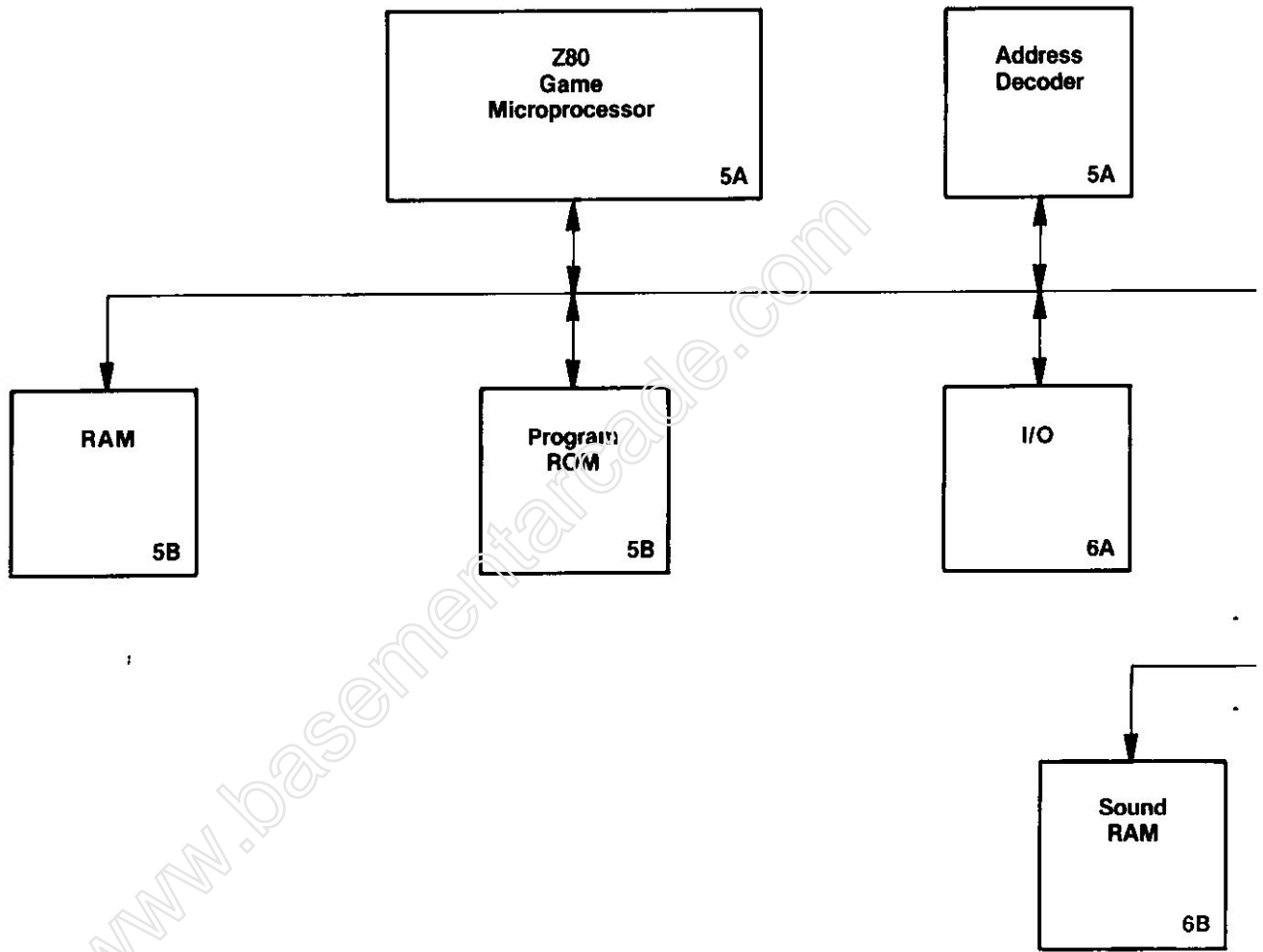
Kangaroo Game Wiring Interfaces

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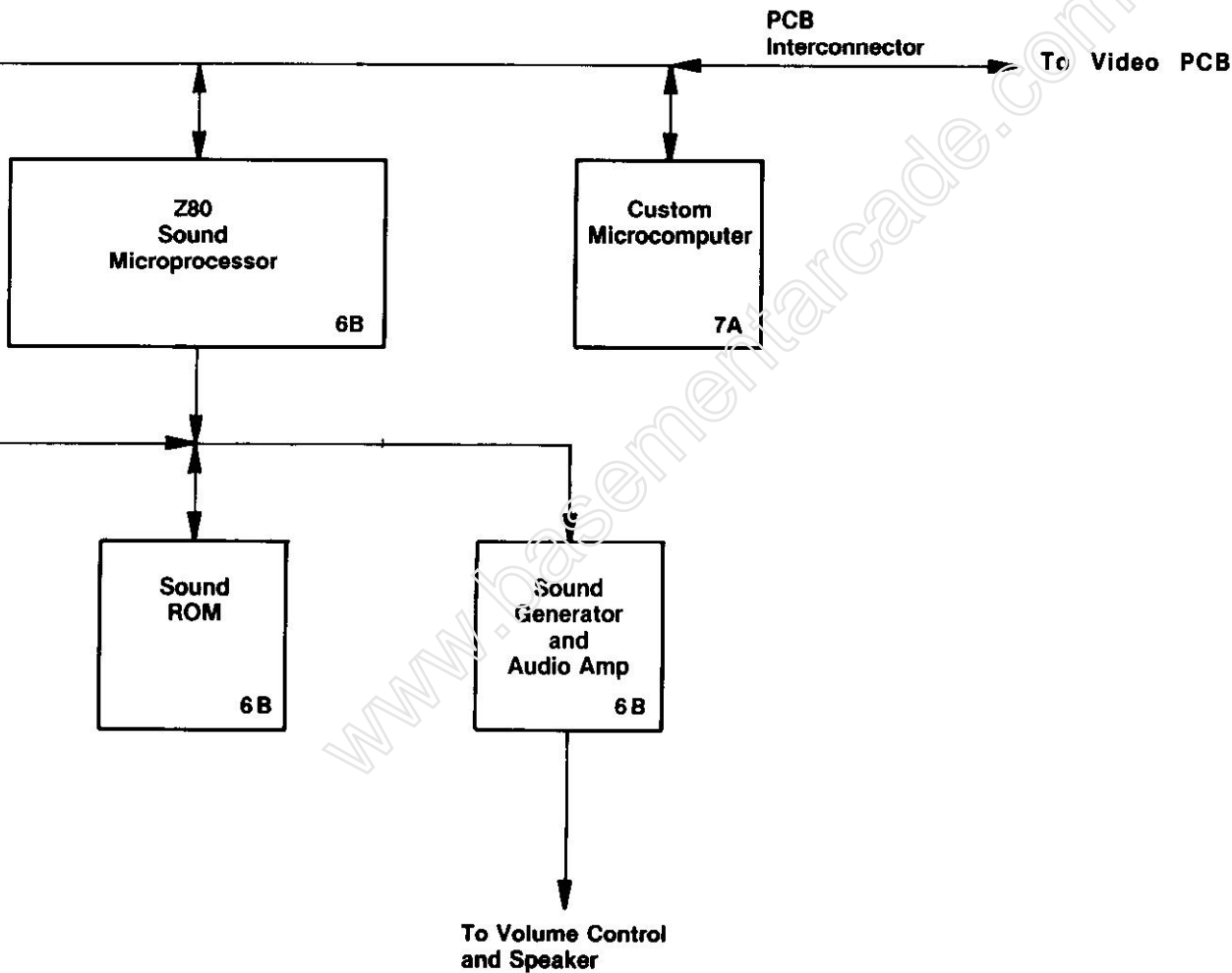
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Block Diagram (CPU PCB)



NOTE


The **service switch**, located on the CPU PCB, allows you to enter credits without tripping the coin counter.



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Kangaroo CPU PCB Schematic Diagram

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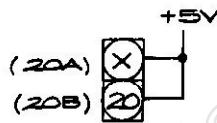
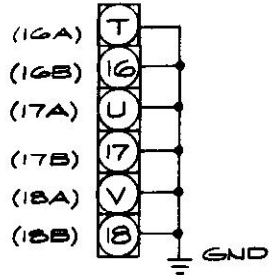
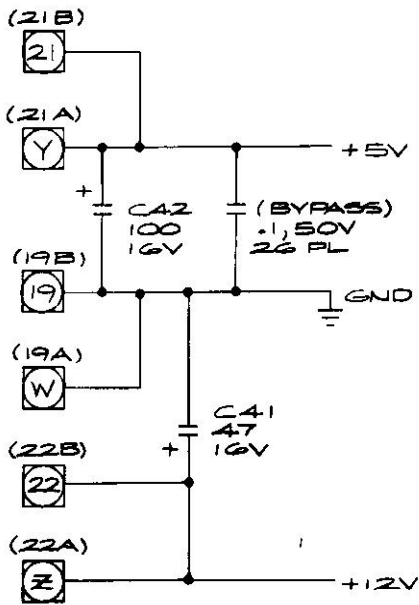
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Memory Map

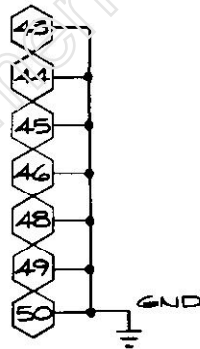
HEXA-DECIMAL ADDRESS	R/W	DATA D7 D6 D5 D4 D3 D2 D1 D0	FUNCTION
Game Microprocessor Memory Space (IC15)			
0000-5FFF	R	D D D D D D D D	Z80 24K Program ROM
E000-E3FF	R/W	D D D D D D D D	1K Working RAM
E400	R	D D D D D D D D	Option Switch
E800	W	D D D D D D D D	Low Byte } Start Address of Data in Picture High Byte } ROM for DMA
E801	W	D D D D D D D D	
E802	W	D D D D D D D D	Low Byte } Start Address in Bit Map RAM (where High Byte } picture is to be written) During DMA
E803	W	D D D D D D D D	
E804	W	D D D D D D D D	Low Byte } Picture Size for DMA High Byte } and DMA Start
E805	W	D D D D D D D D	
E806	W	D D D D D D D D	Vertical Start Address in Bit Map
E807	W	D D D D D D D D	Horizontal Start Address in Bit Map
E808	W	D D D D D D D D	Bank Select Latch
E809	W	D D D D D D D D	A & B Bit Map Control Latch (A = playfield, B = motion)
E80A	W	D D D D D D D D	Color-Shading Latch
EC00	W	D D D D D D D D	Sound DATA to Sound Microprocessor
EC00	R	D D D D D D D D	Utility Coin Switch
EC00	R	D D D D D D D D	1 Player Start
EC00	R	D D D D D D D D	2 Player Start
EC00	R	D D D D D D D D	Left Coin Input
EC00	R	D D D D D D D D	Right Coin Input
ED00	W	D D D D D D D D	Coin Counter 1
ED00	W	D D D D D D D D	Coin Counter 2 (European games)
ED00	R	D D D D D D D D	Player 1 Right
ED00	R	D D D D D D D D	Player 1 Left
ED00	R	D D D D D D D D	Player 1 Up
ED00	R	D D D D D D D D	Player 1 Down
ED00	R	D D D D D D D D	Player 1 Punch
EE00	R	D D D D D D D D	Player 2 Right
EE00	R	D D D D D D D D	Player 2 Left
EE00	R	D D D D D D D D	Player 2 Up
EE00	R	D D D D D D D D	Player 2 Down
EE00	R	D D D D D D D D	Player 2 Punch
EFXx	W	D D D D D D D D	Output to Custom Microcomputer
EFXx	R	D D D D D D D D	Input from Custom Microcomputer
Sound Microprocessor Memory Space (IC34)			
0000-0FFF	R	D D D D D D D D	4K Program ROM
4000-43FF	R/W	D D D D D D D D	1K Working RAM
6000	R	D D D D D D D D	Read DATA from Game Microprocessor
7000	W	D D D D D D D D	Write to Sound Chip (GI-AY-3-8910)
8000	R	D D D D D D D D	Read from Sound Chip

CPU Power Input



NOTES:

- 1.  = CONNECTOR CN2
- 2.  = CONNECTOR CN1



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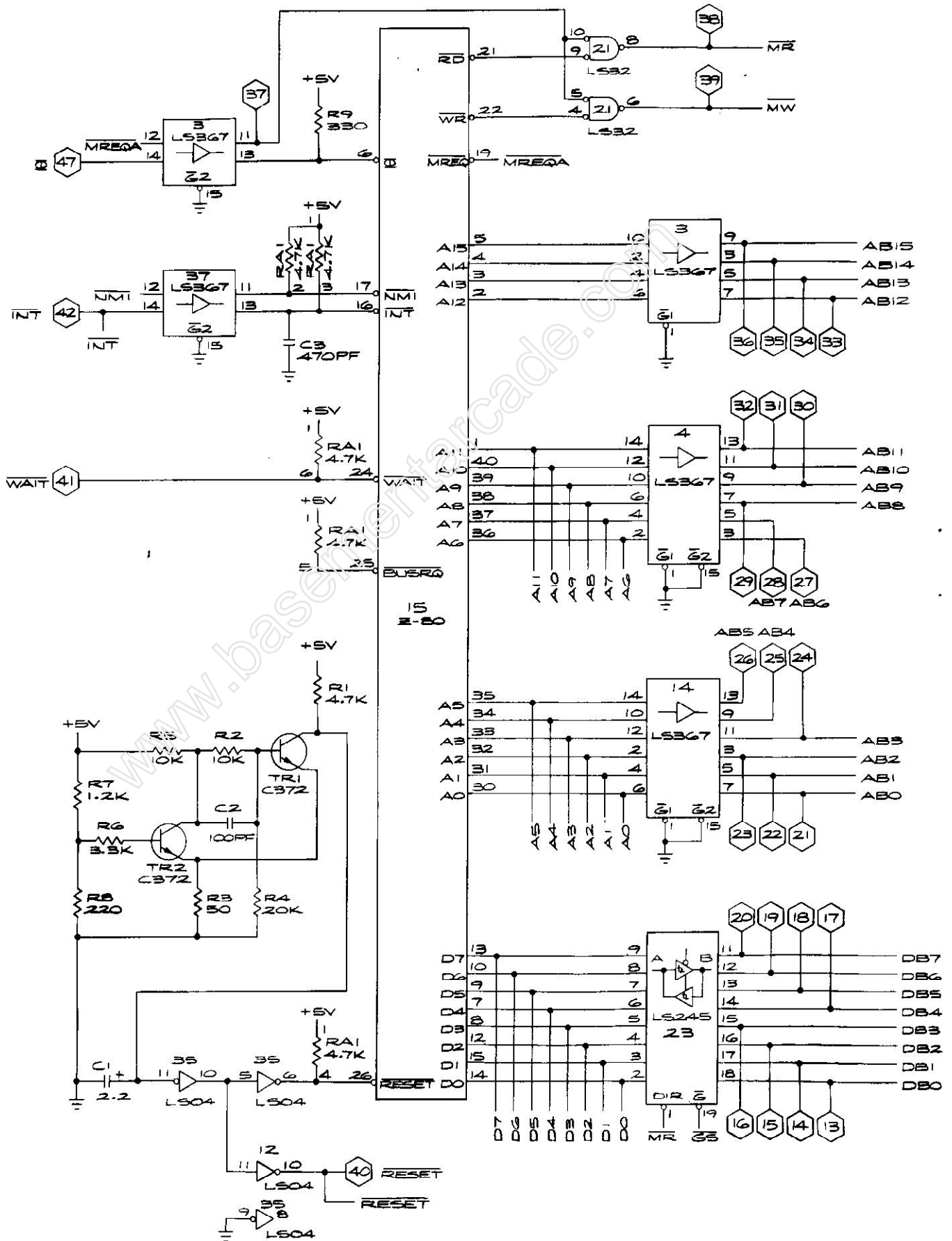
Kangaroo CPU PCB Schematic Diagram

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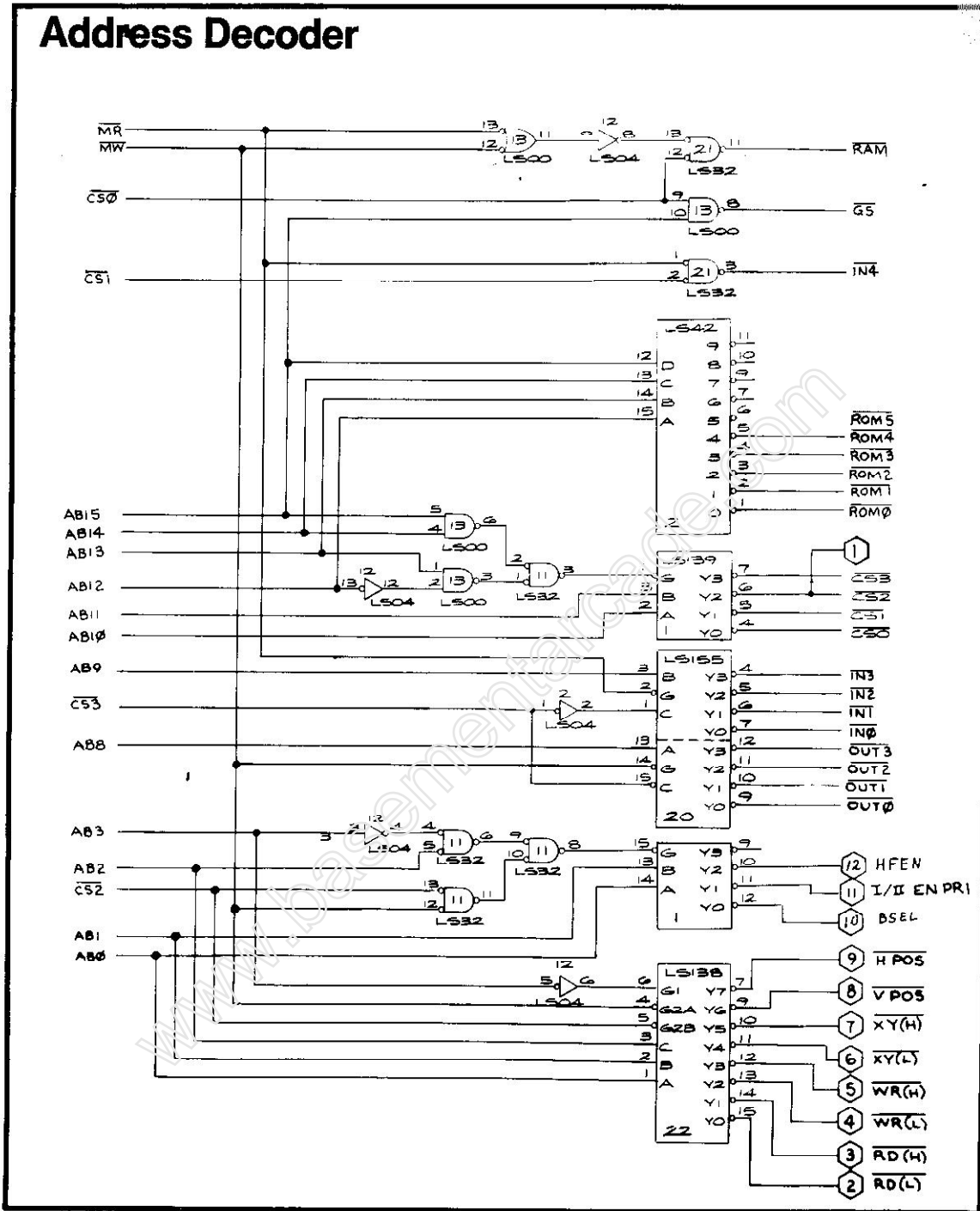
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Game Microprocessor



Address Decoder



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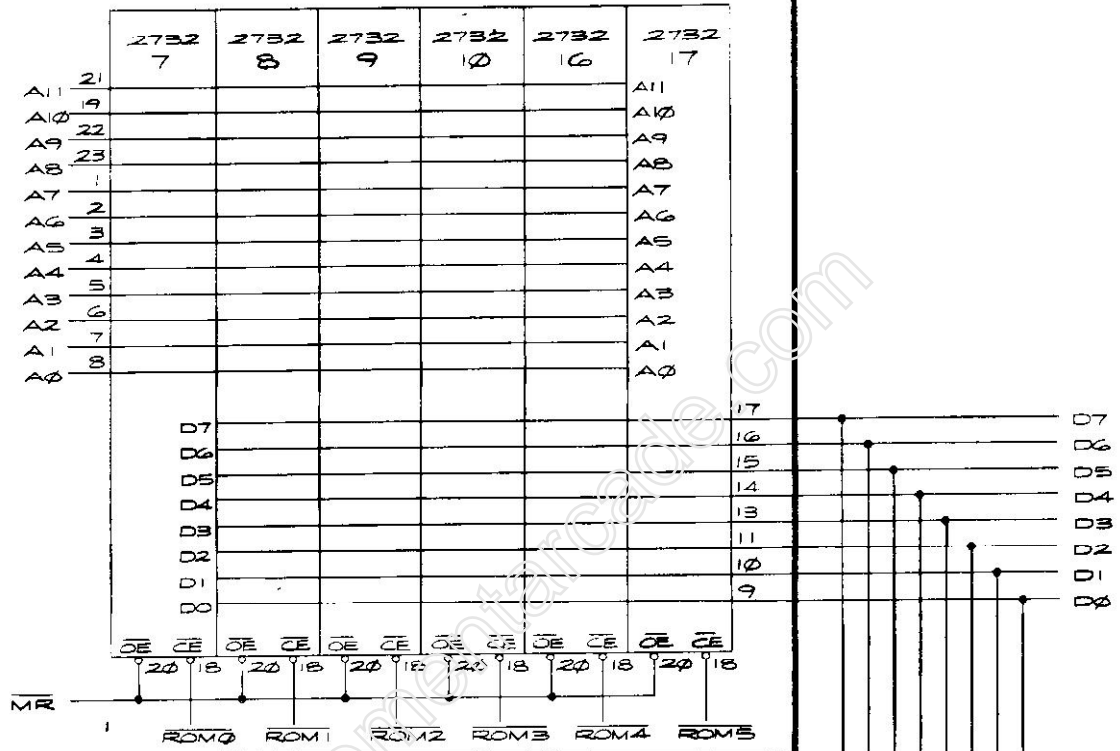
Kangaroo CPU PCB Schematic Diagram

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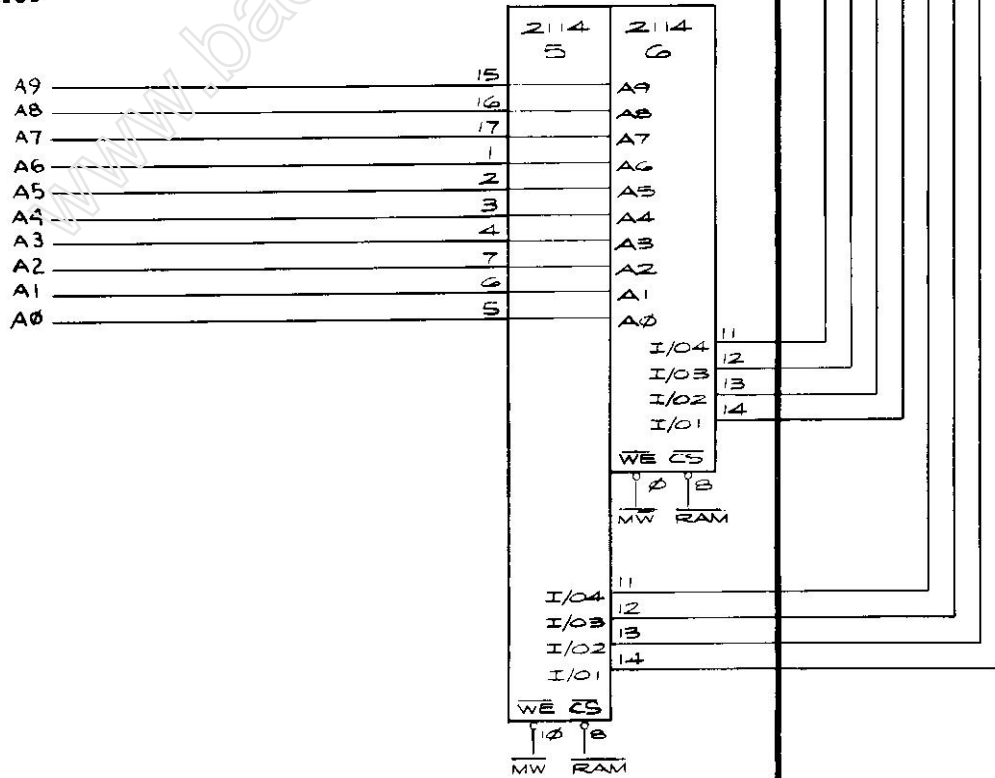
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Program ROM



RAM



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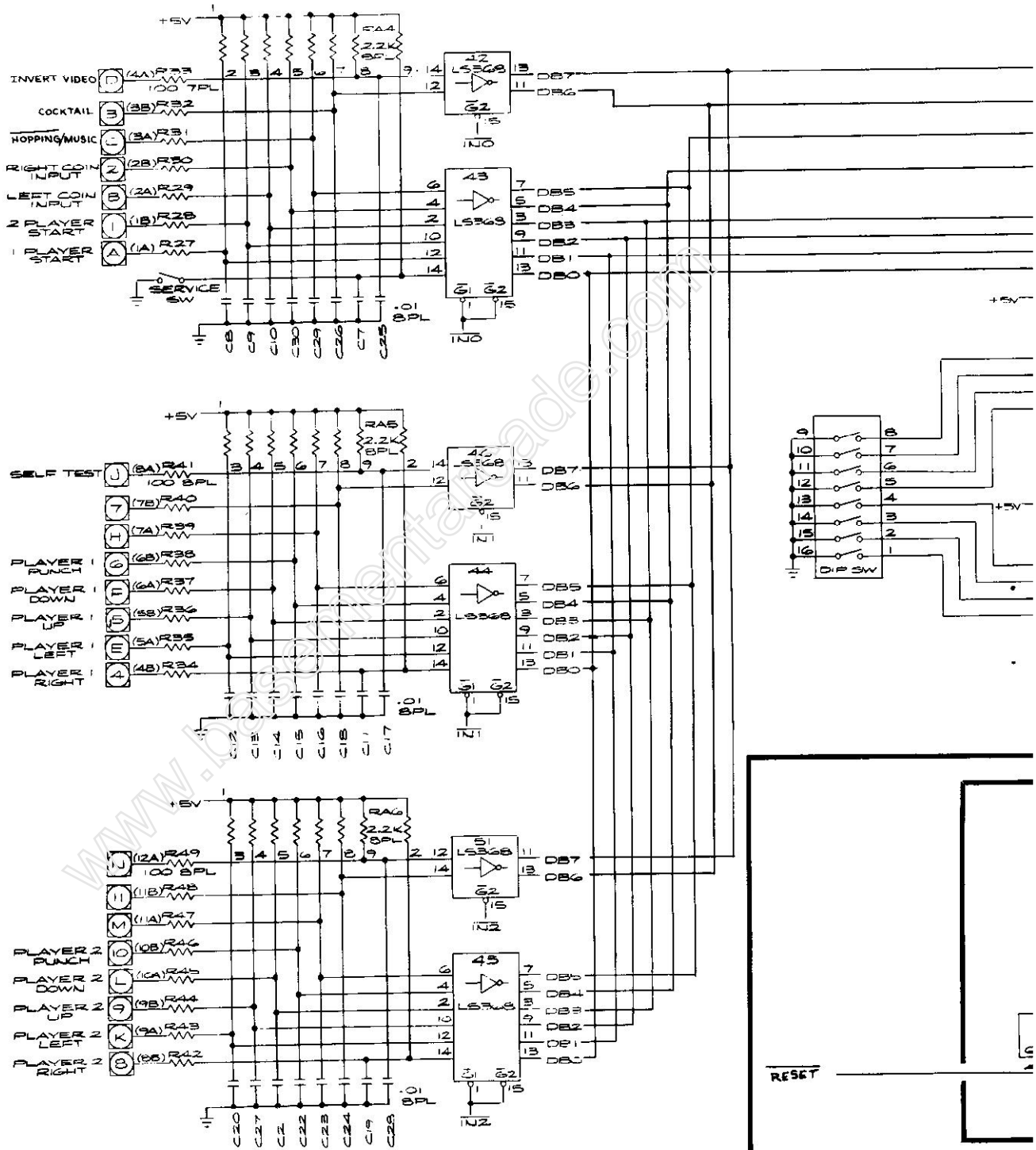
Kangaroo CPU PCB Schematic Diagram

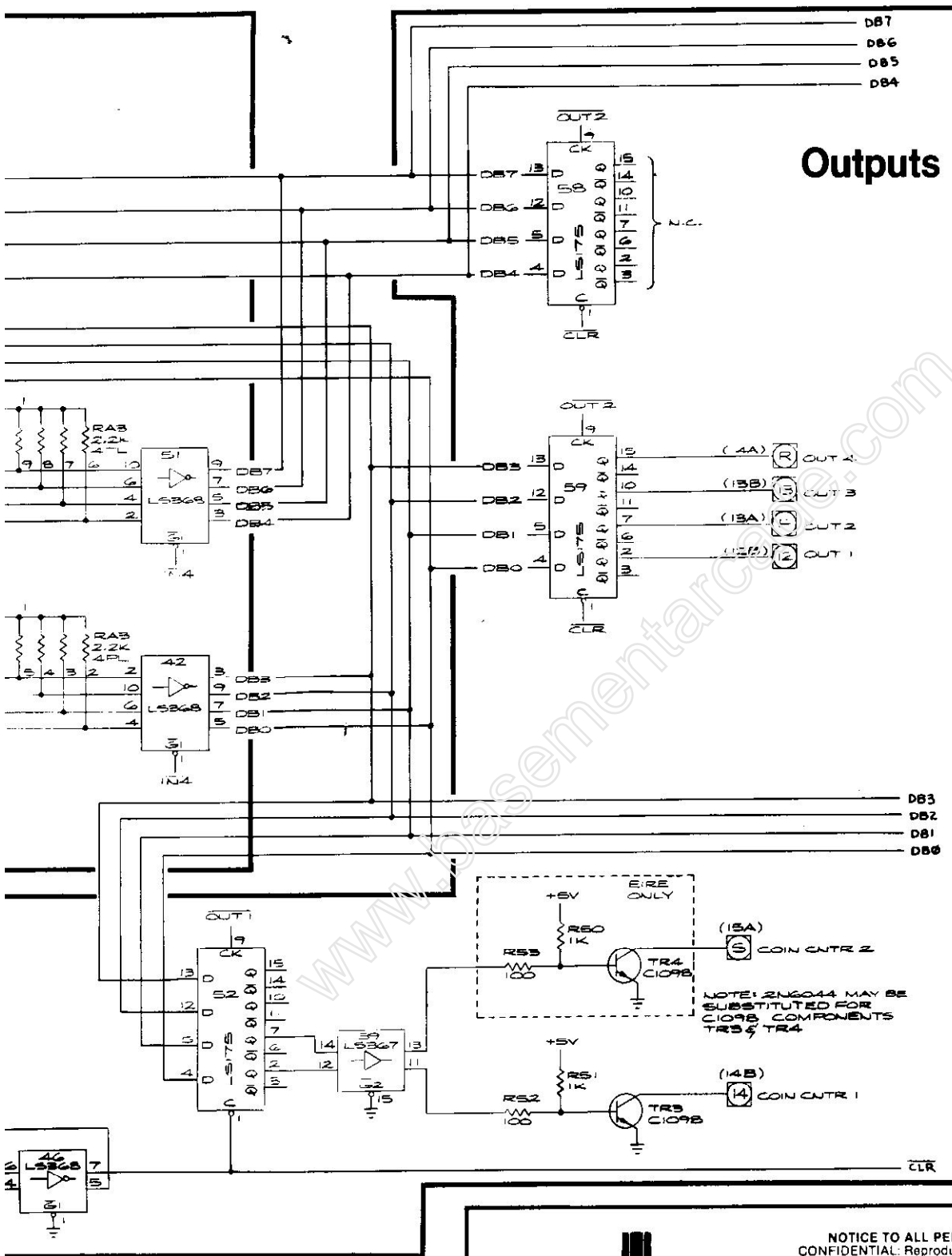
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Inputs

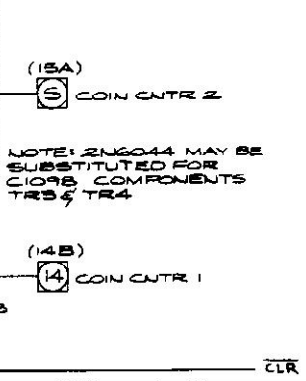




Outputs

DB7
DB6
DB5
DB4

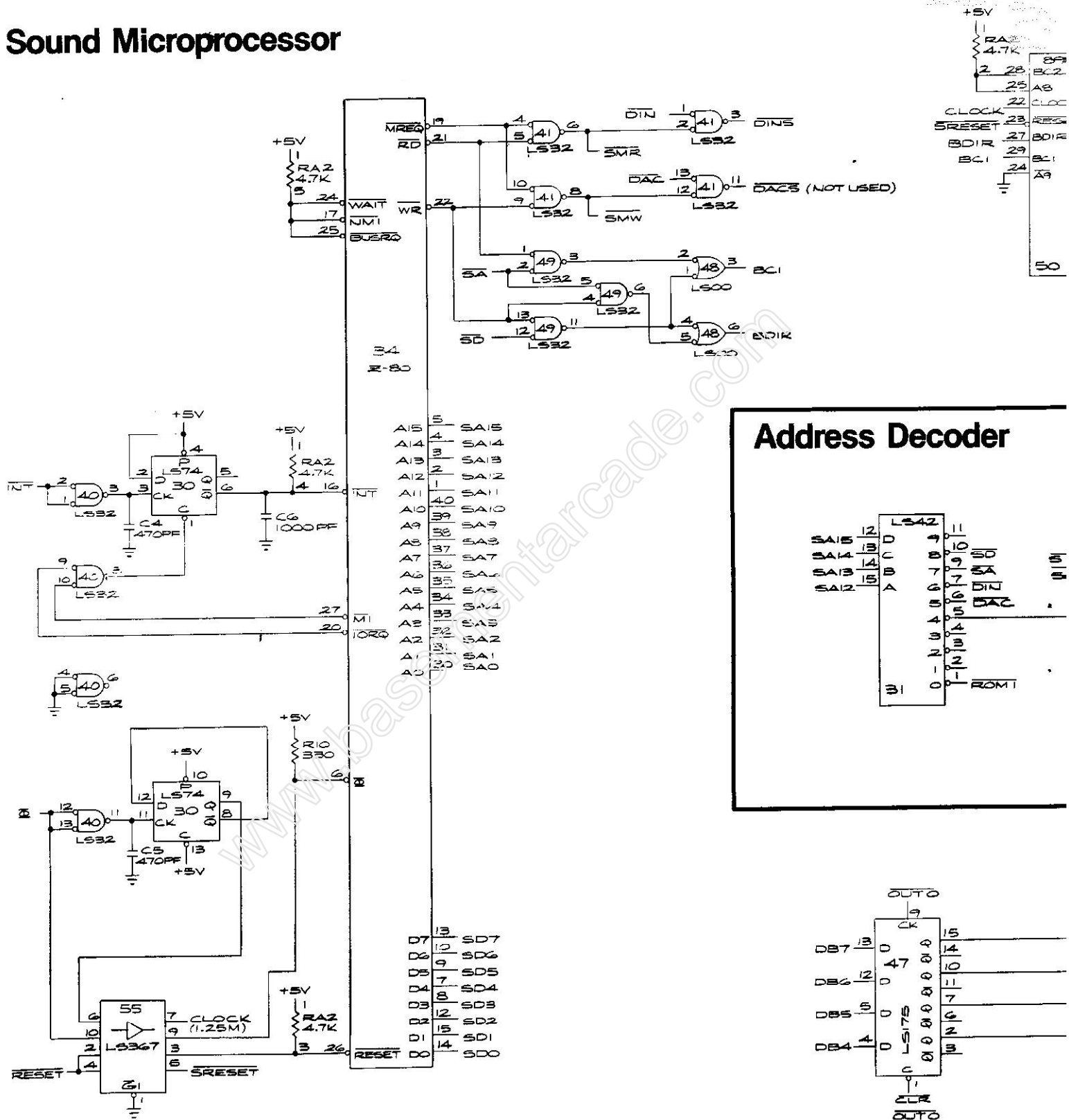
DB3
DB2
DB1
DB0



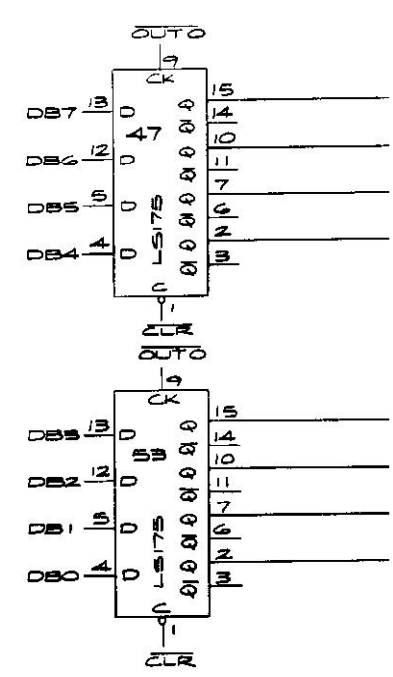
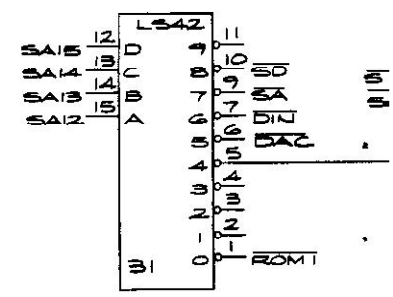
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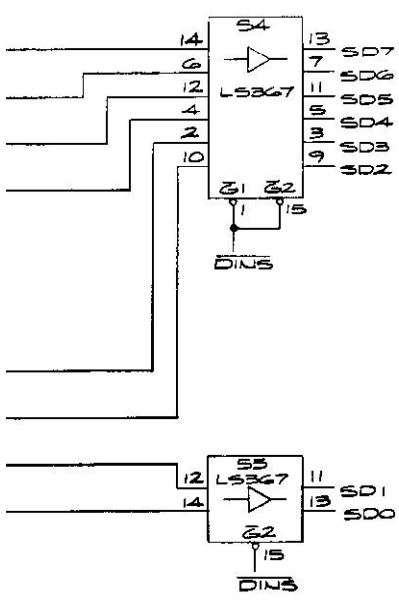
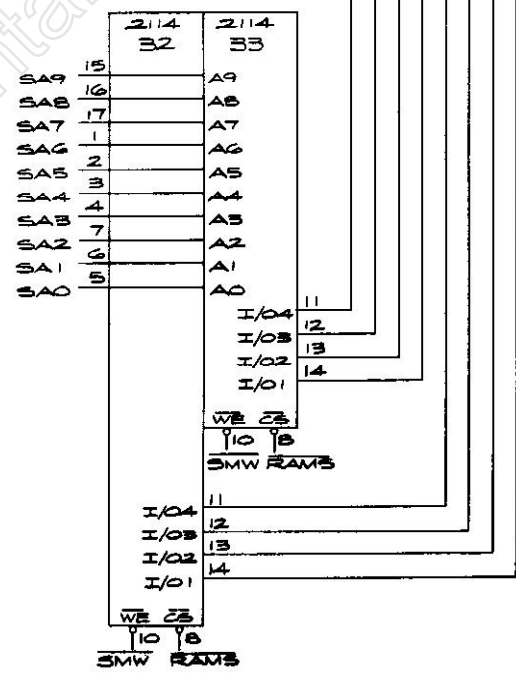
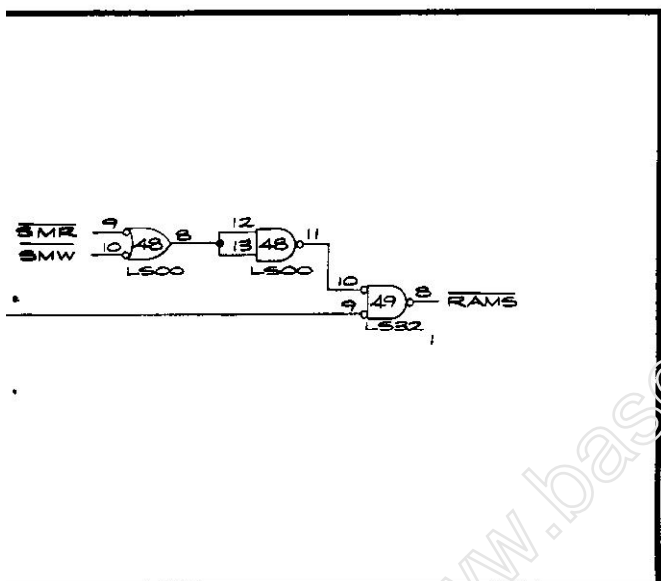
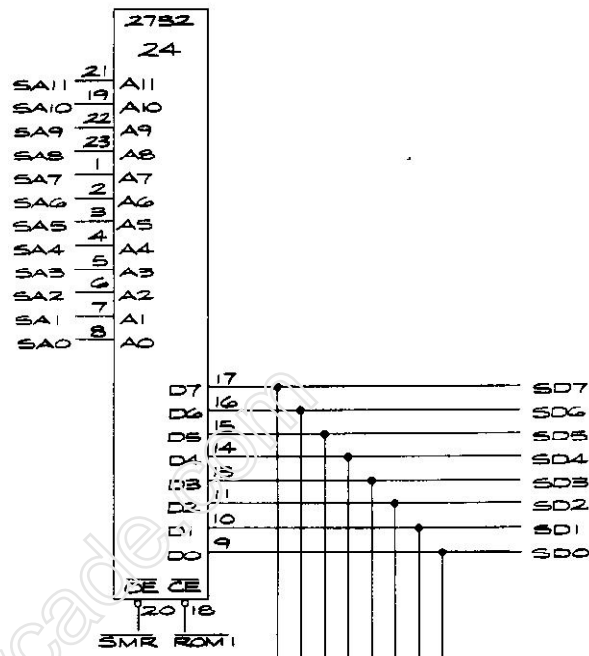
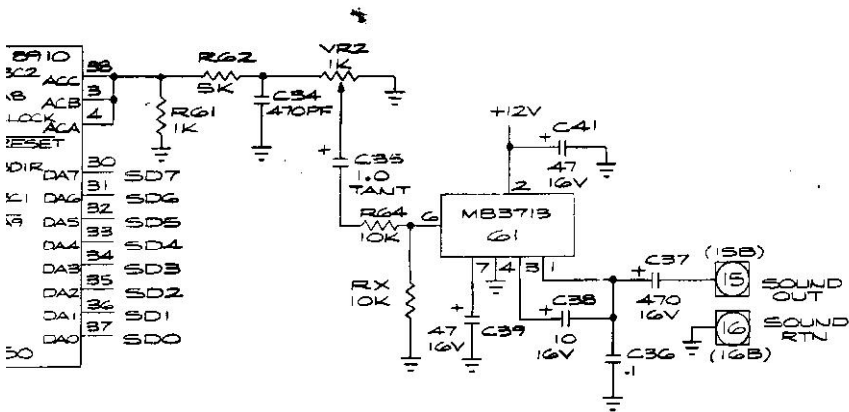
Kangaroo CPU PCB Schematic Diagram


Sound Microprocessor



Address Decoder








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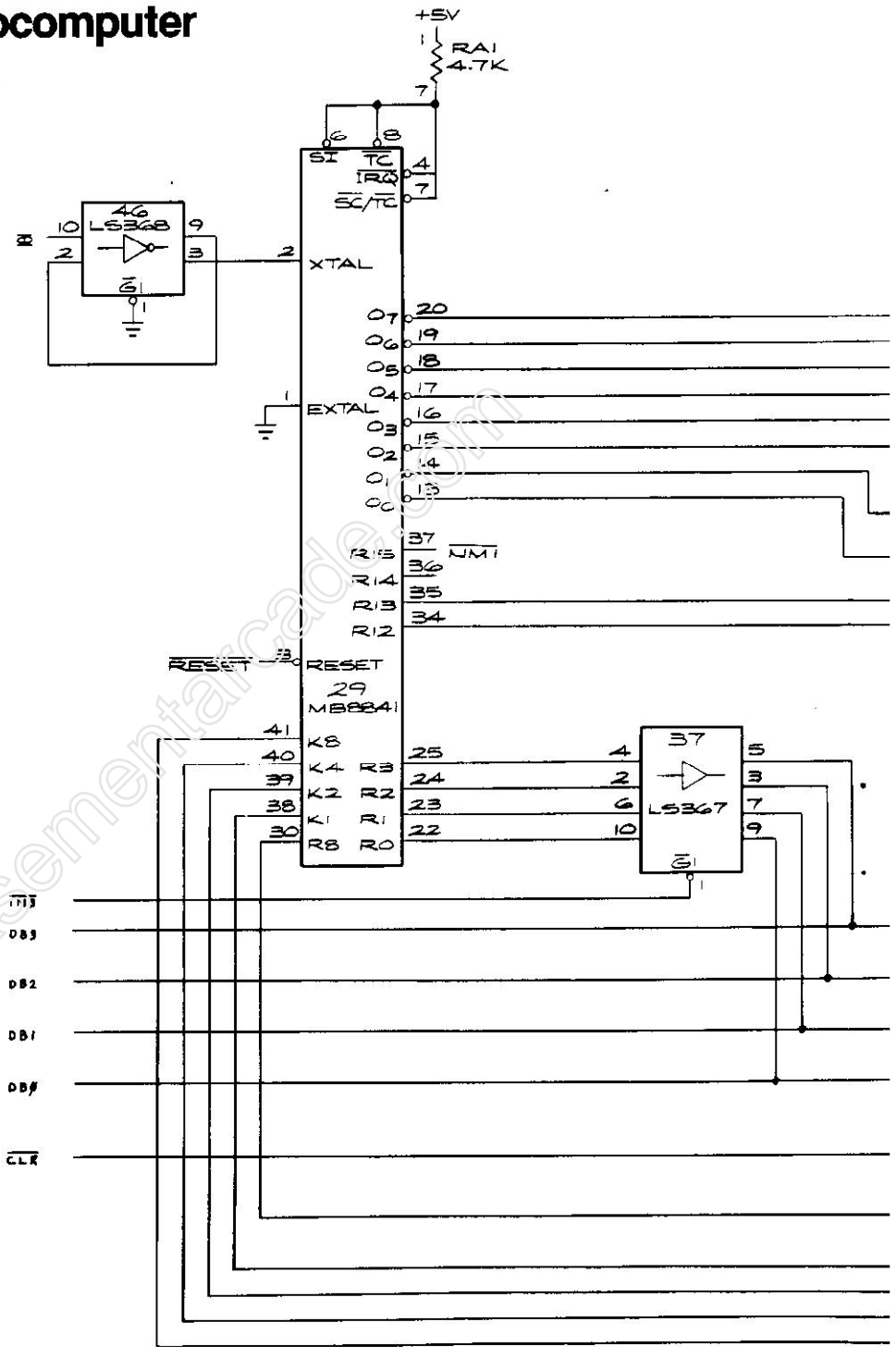
Kangaroo CPU PCB Schematic Diagram

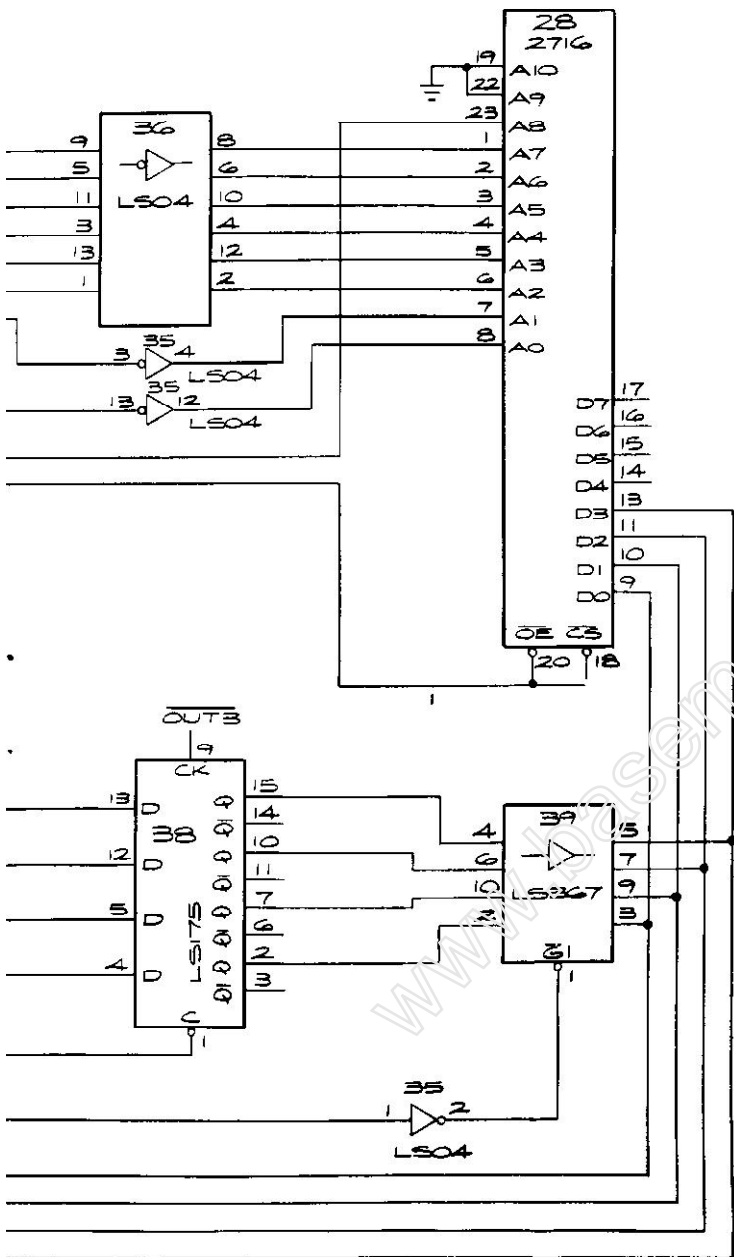
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Custom Microcomputer

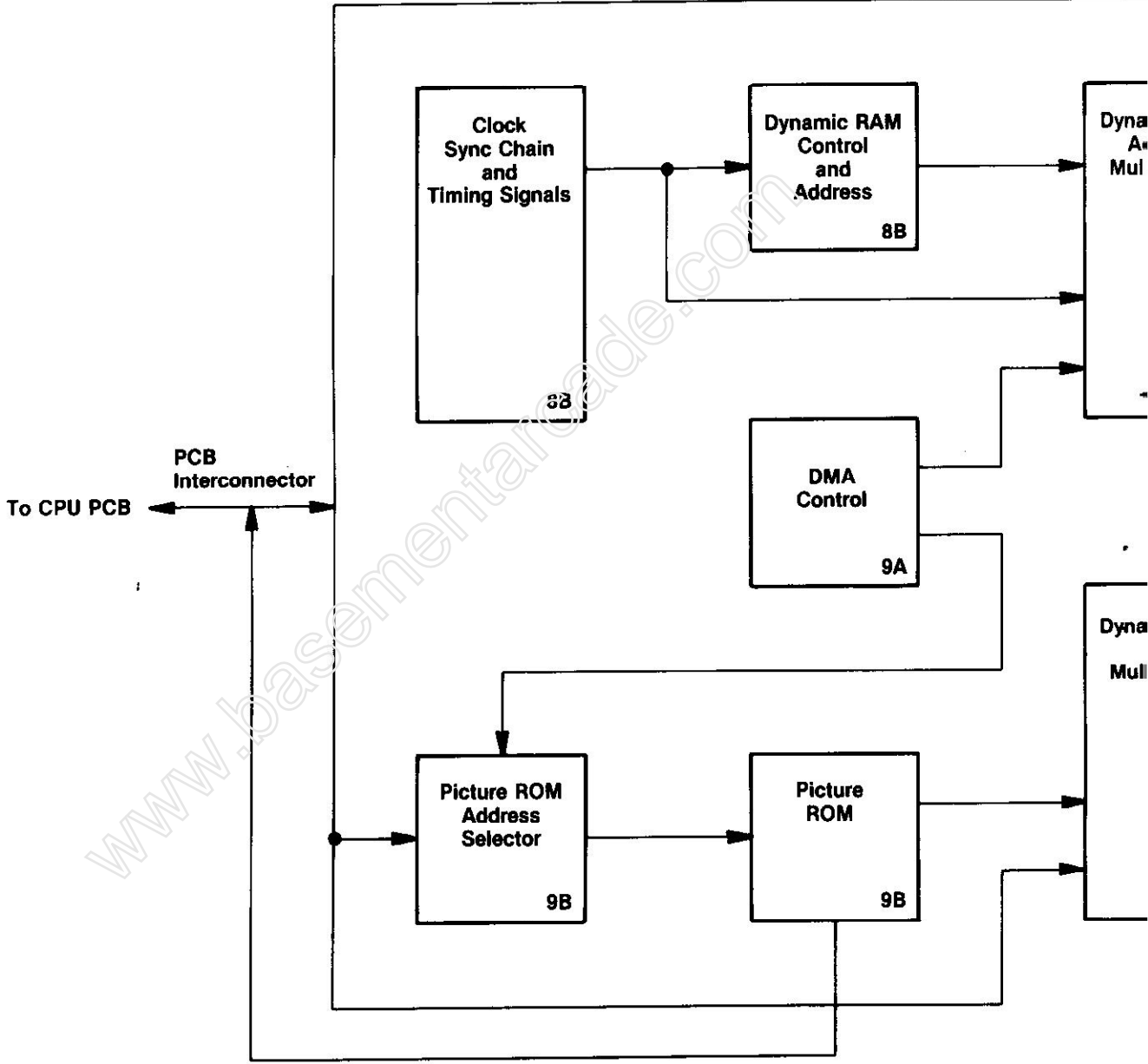


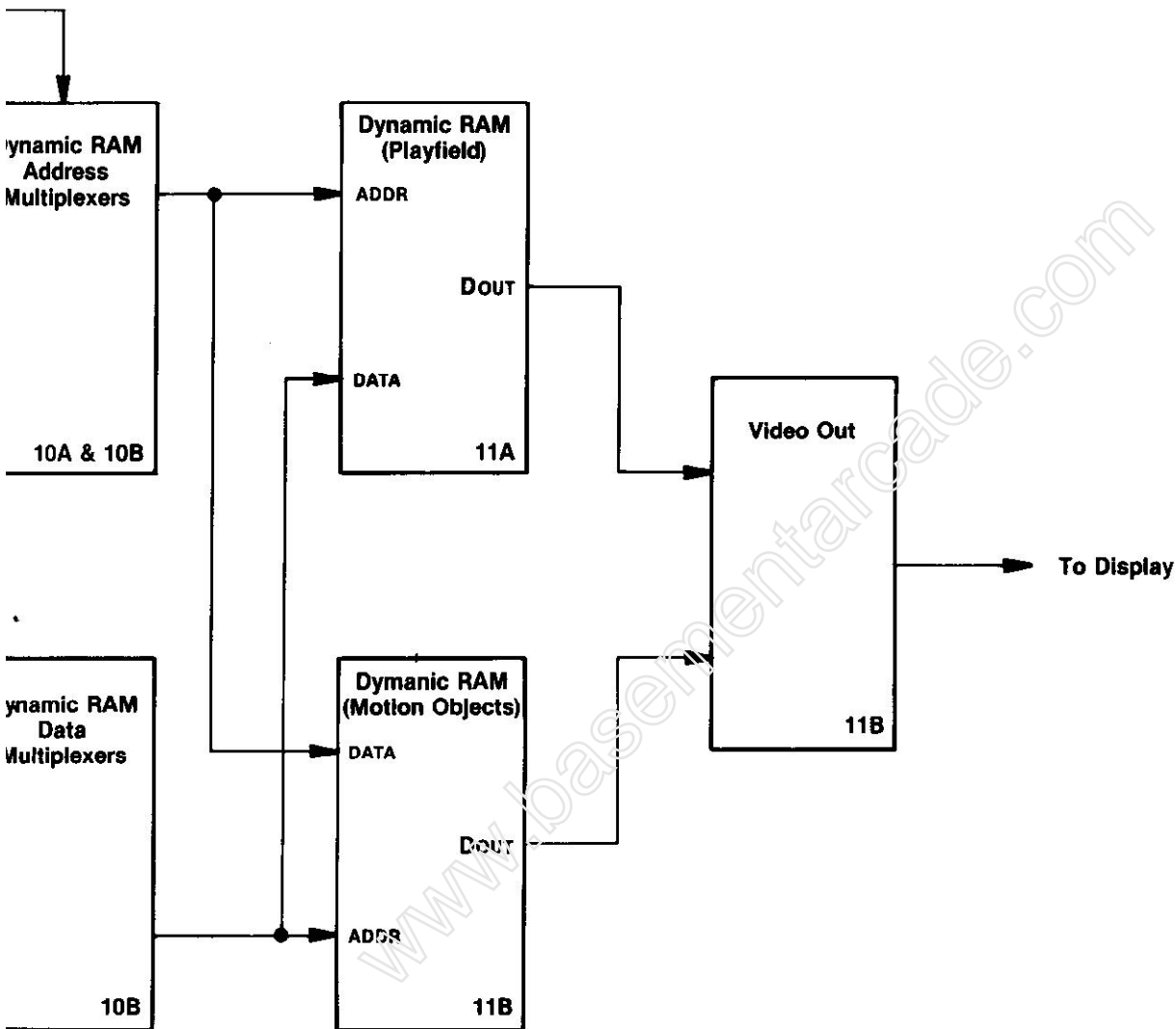


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Kangaroo CPU PCB Schematic Diagram

Block Diagram (Video PCB)





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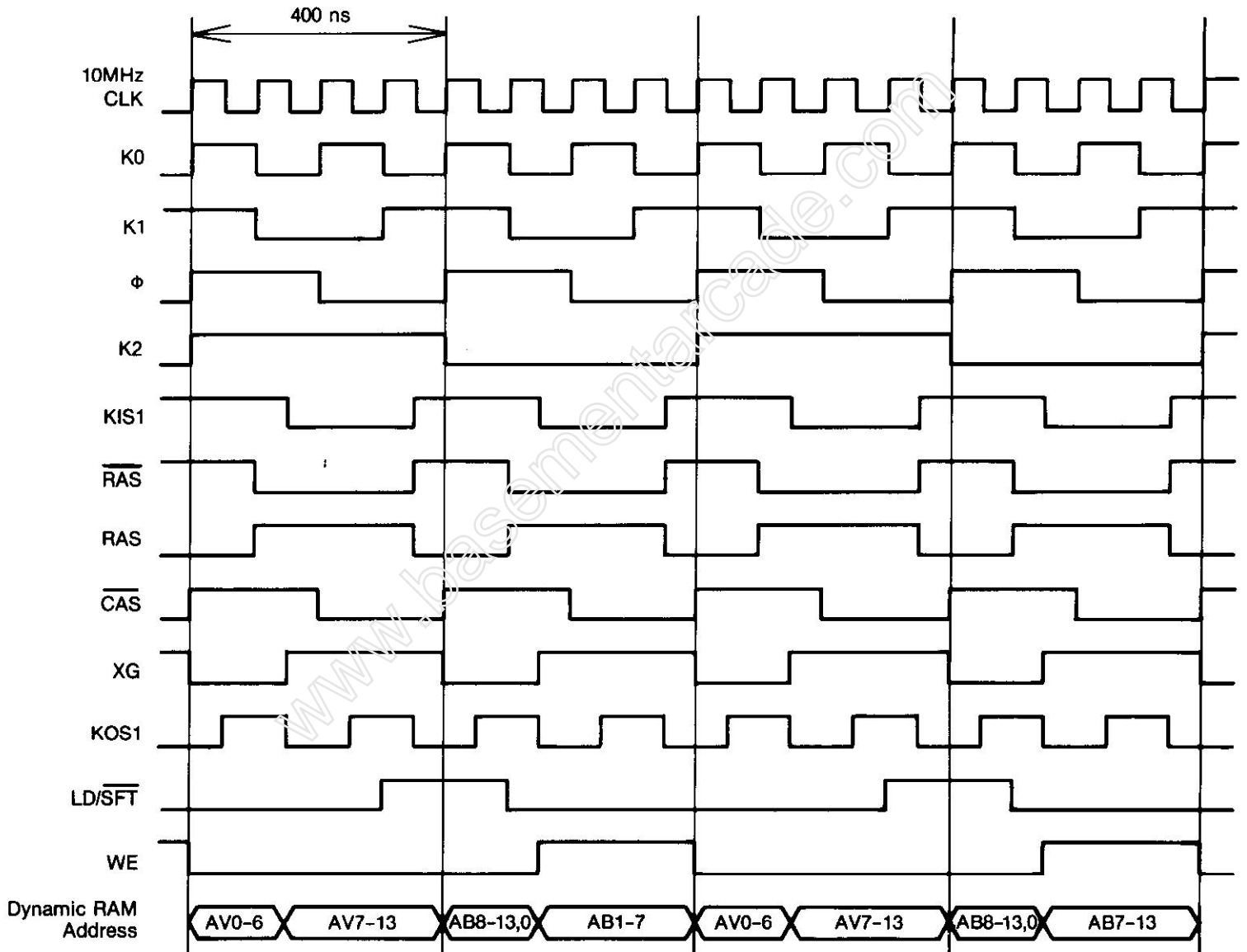
Kangaroo Video PCB Schematic Diagram

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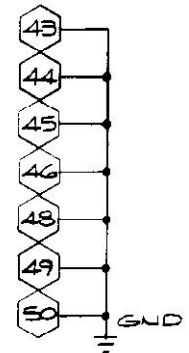
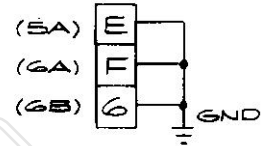
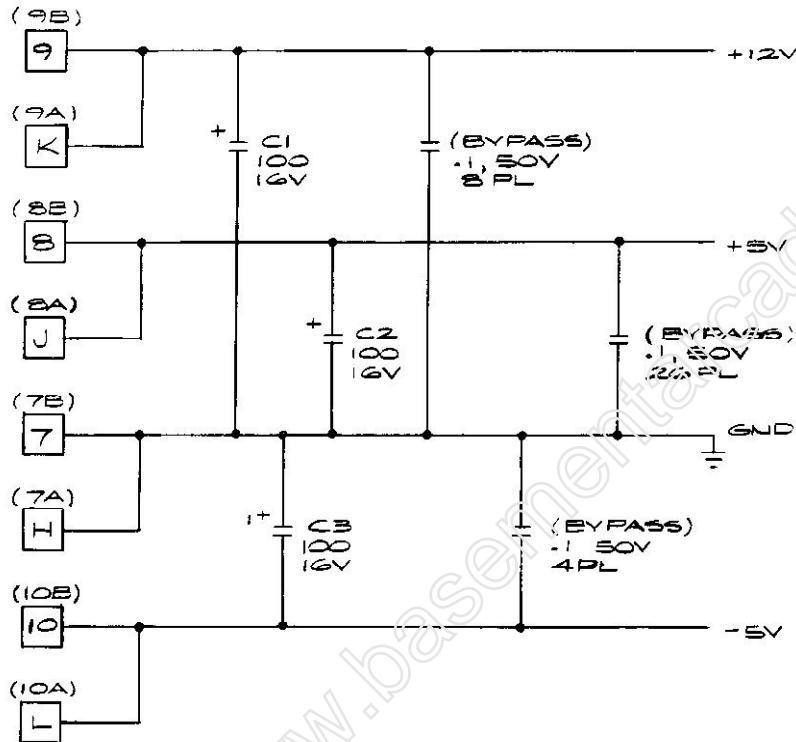
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Dynamic RAM Timing Diagram (Video PCB)



Video Power Input



NOTES:

1.  = CONNECTOR CN1
2.  = CONNECTOR CN4



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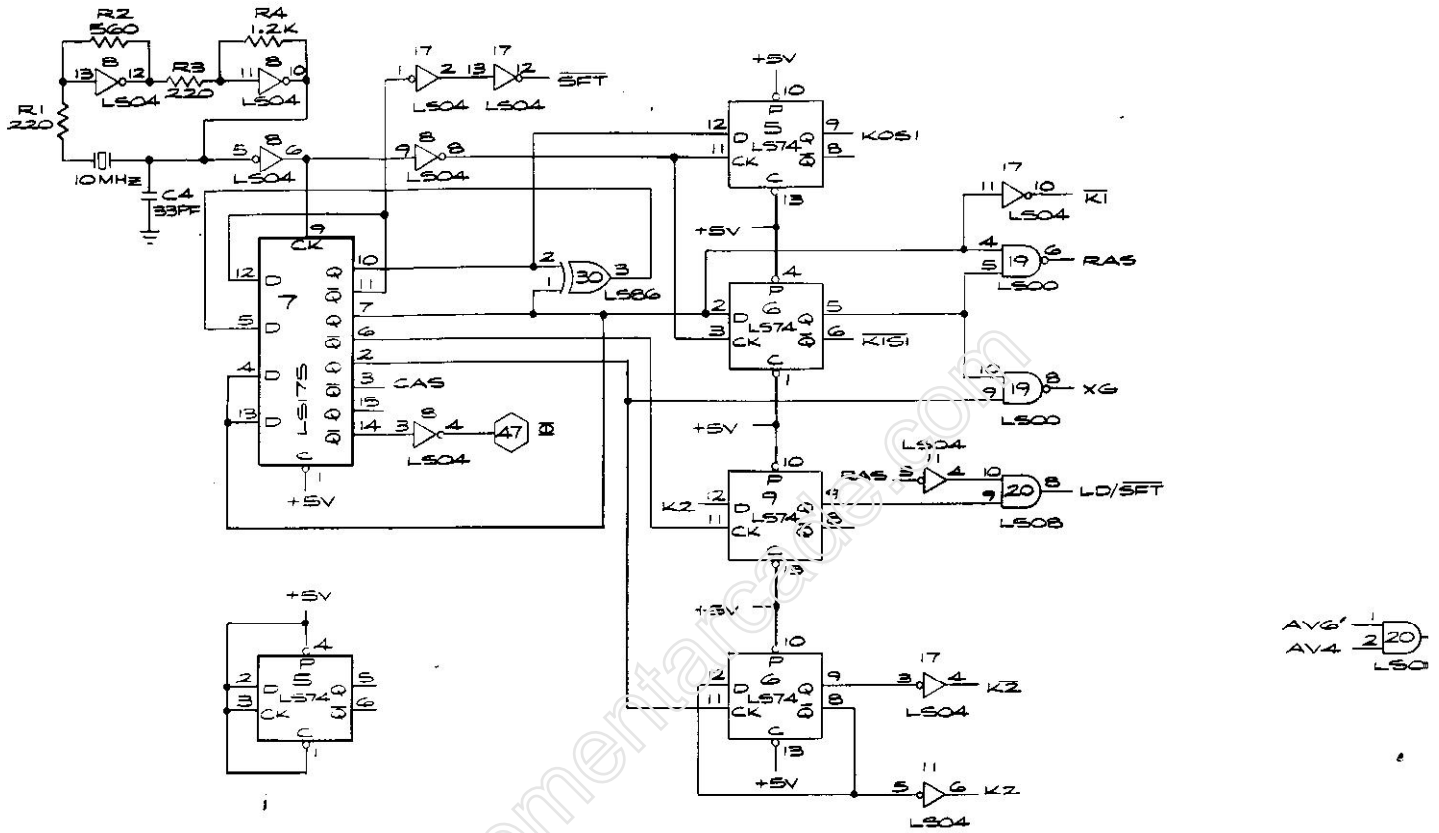
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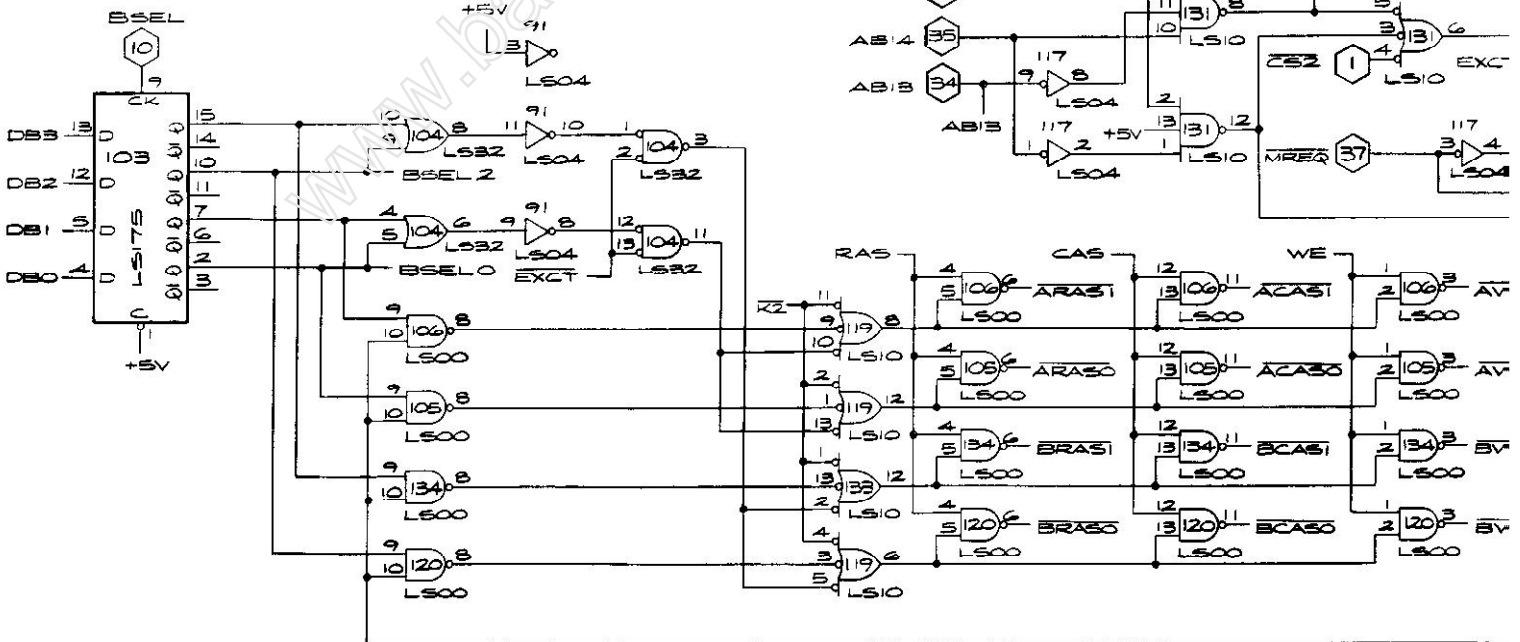
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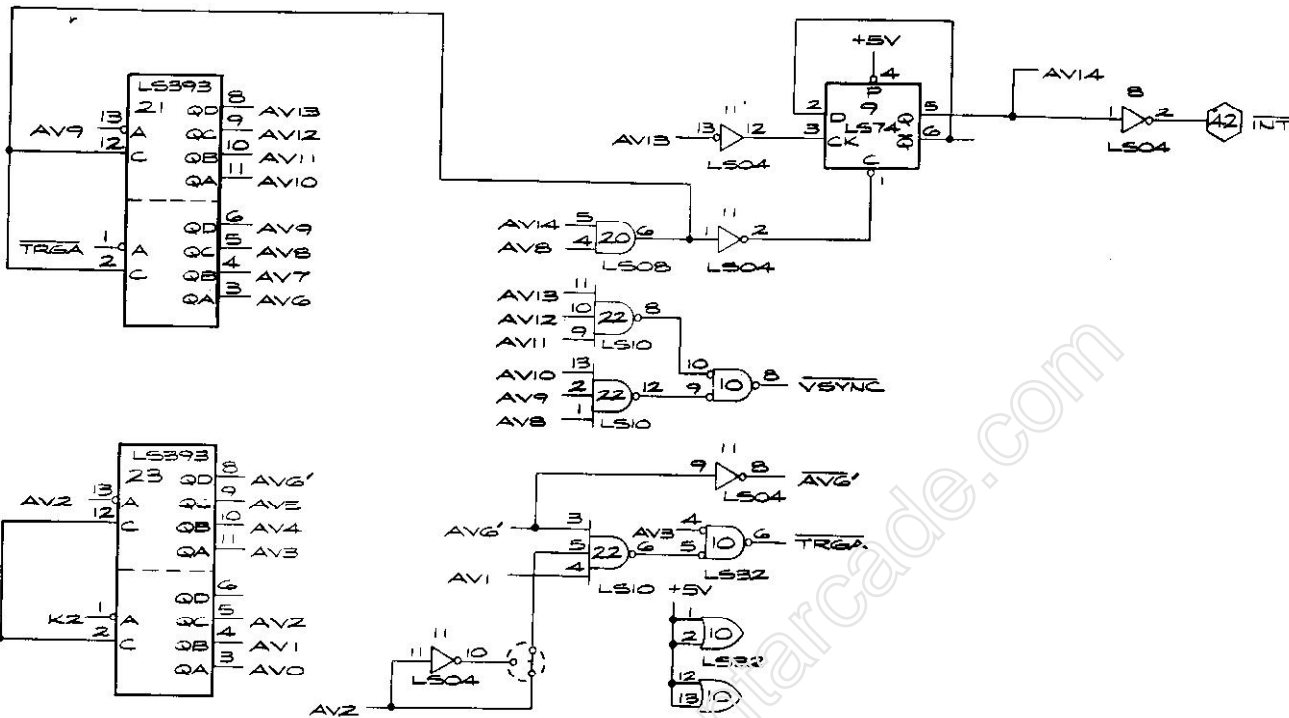
Clock, Sync Chain, and T



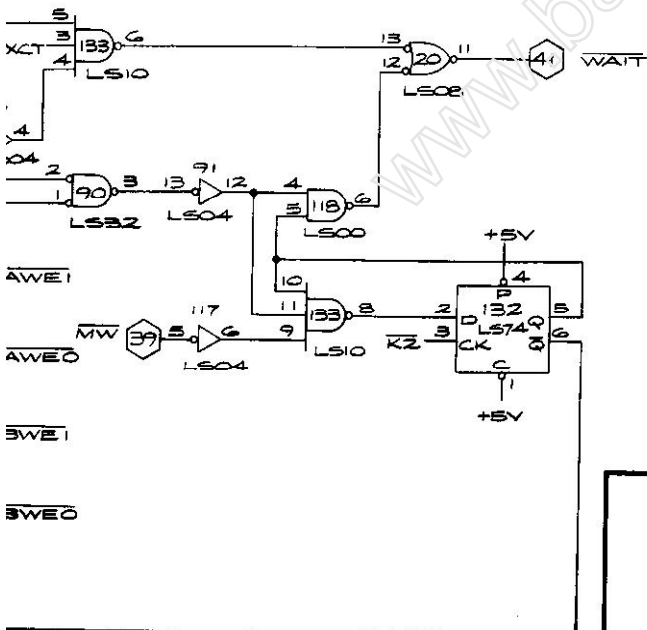
Dynamic RAM Control



Timing Signals



Address Decoding



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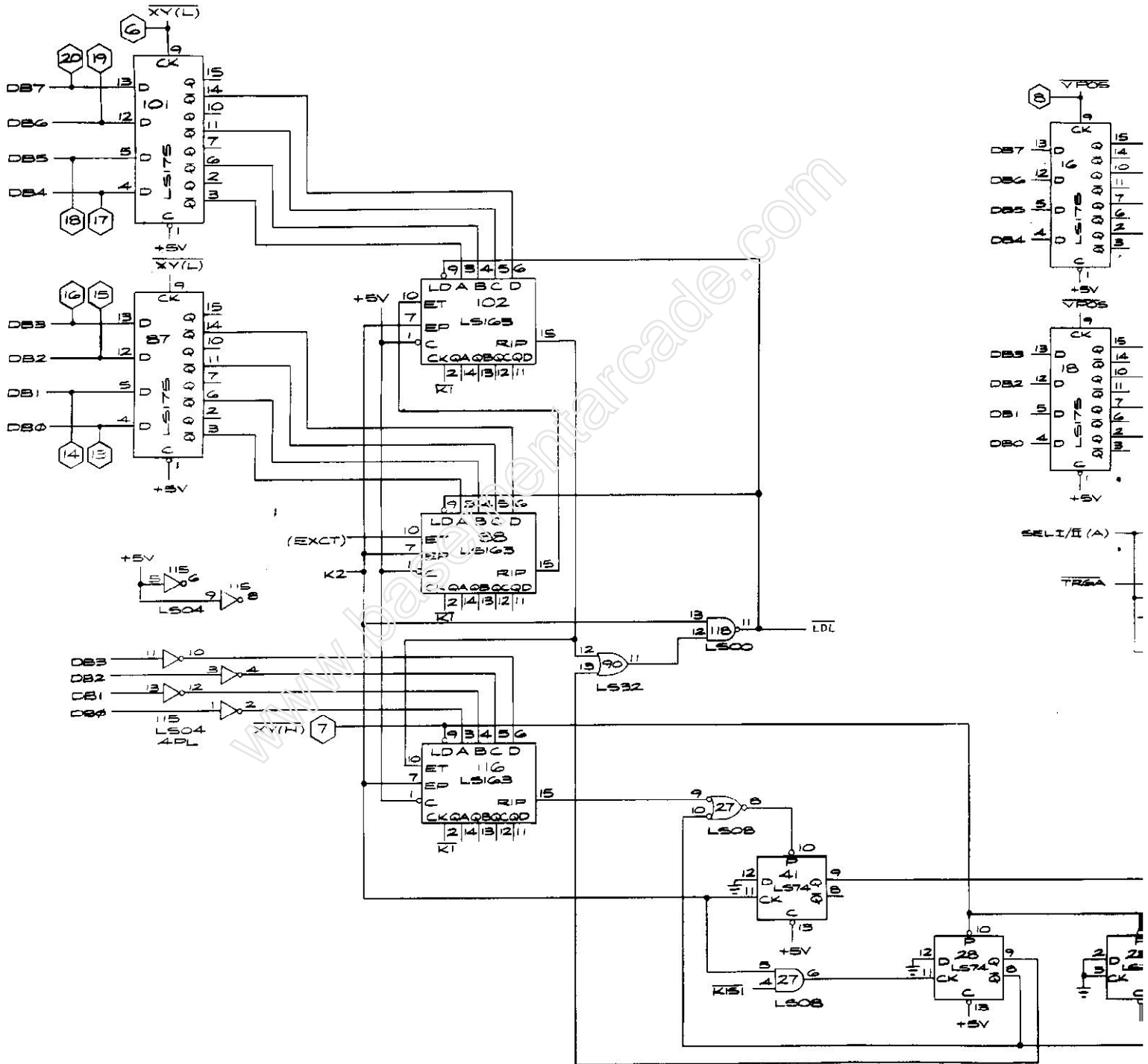
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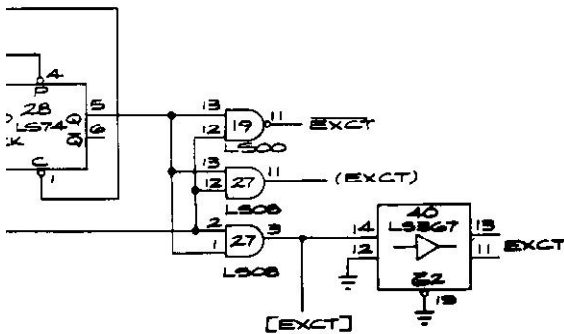
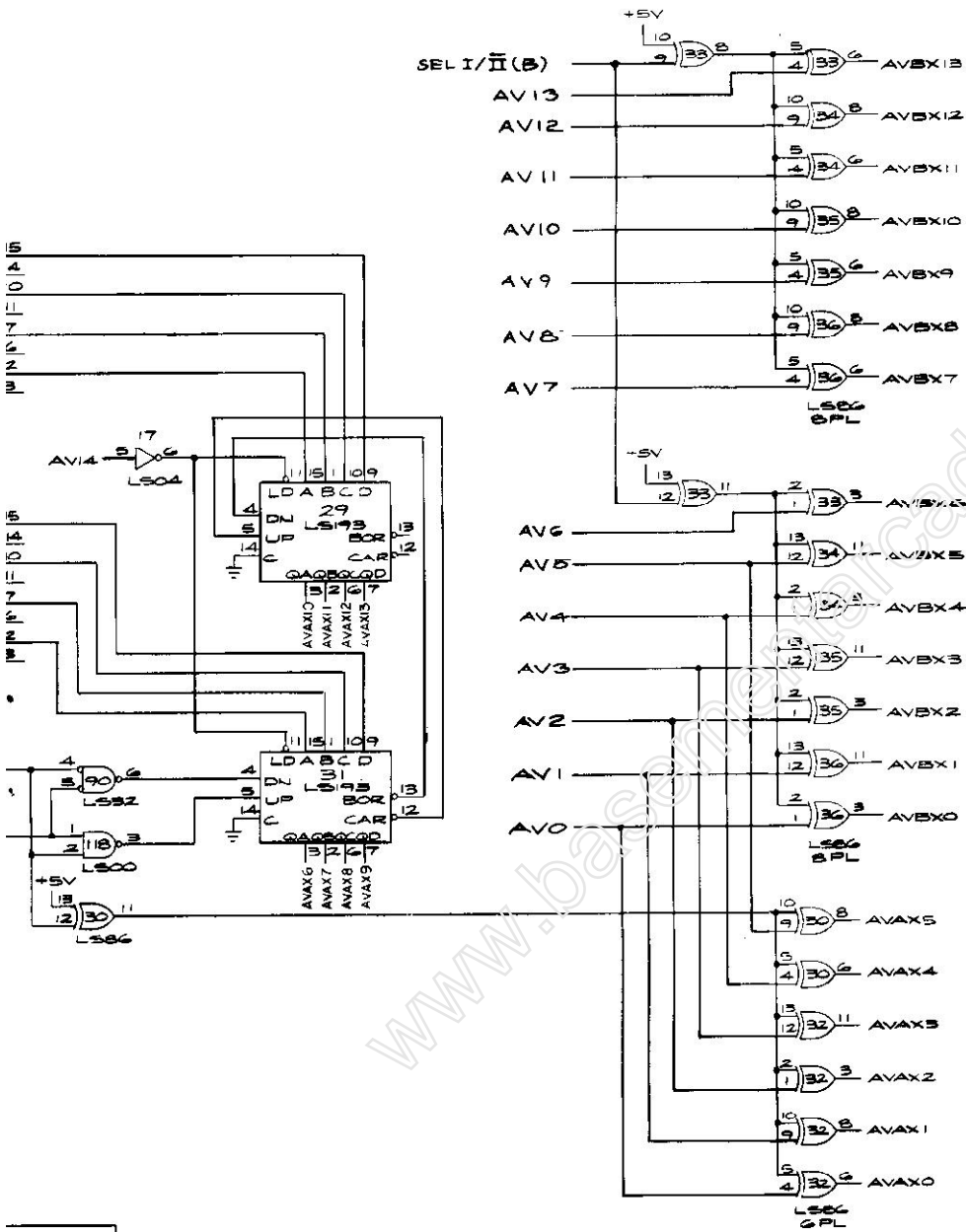
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DMA Control



Dynamic RAM Video Address and Flip



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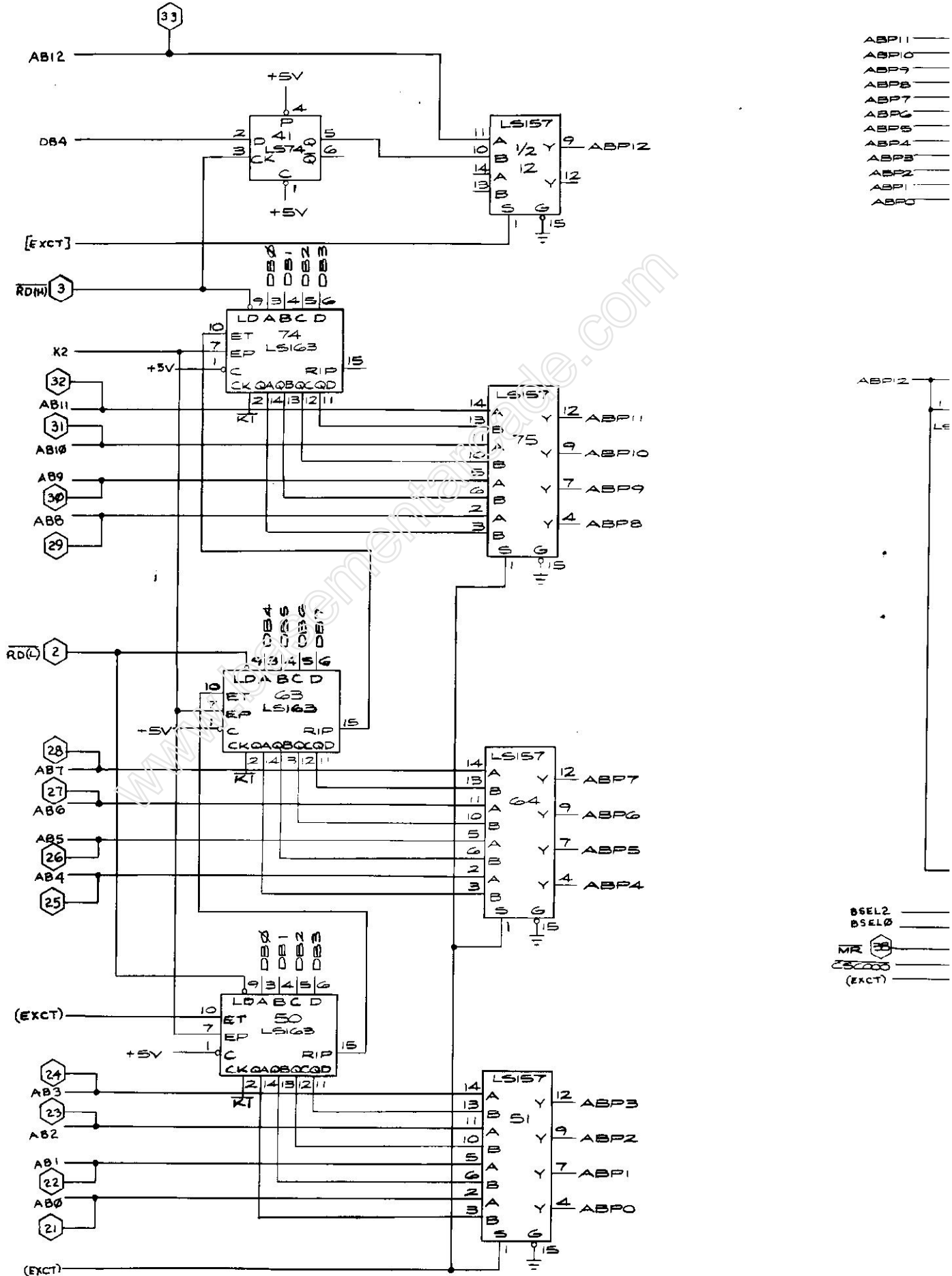
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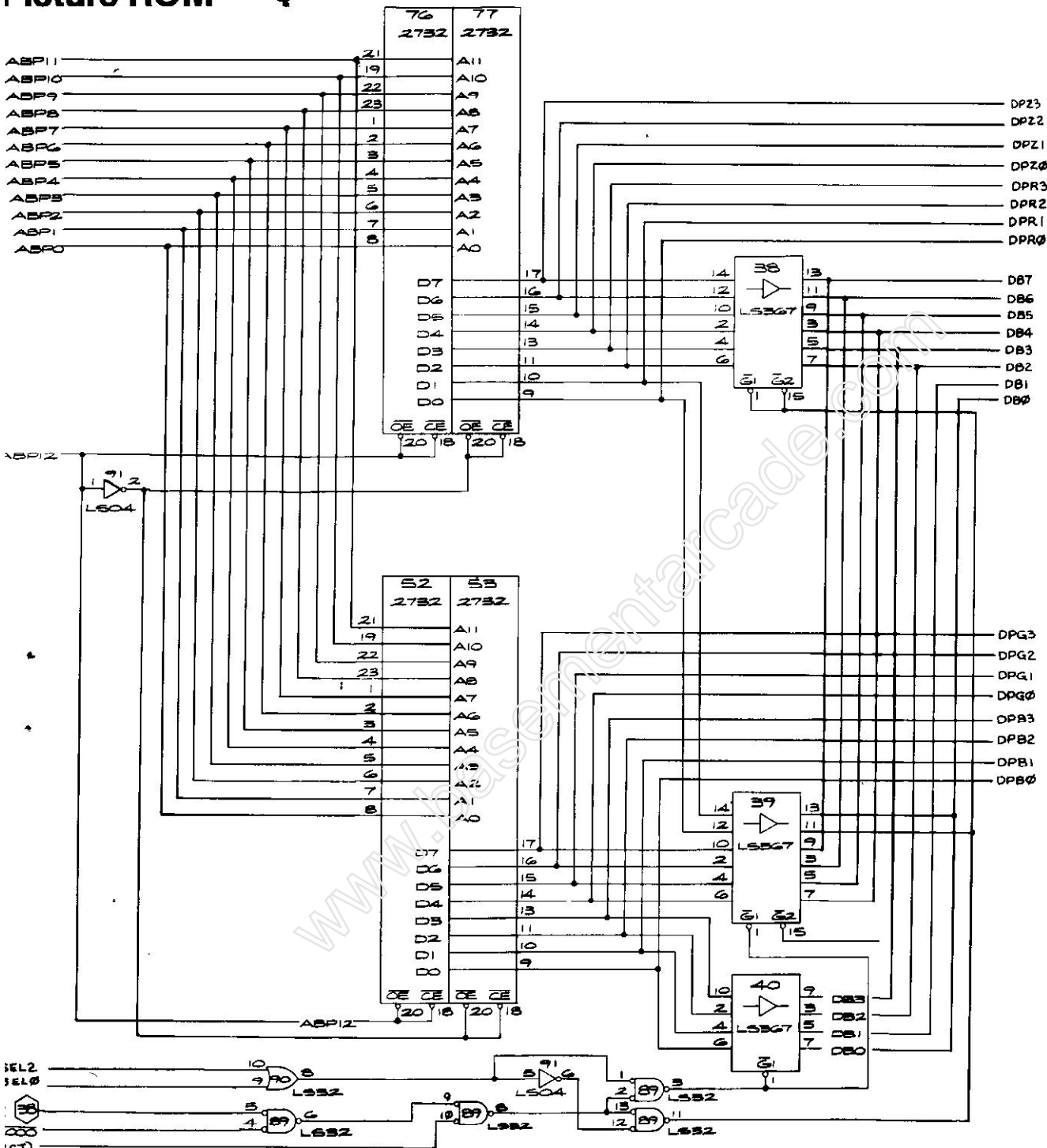
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Picture ROM Address Selector

Pictur



Picture ROM



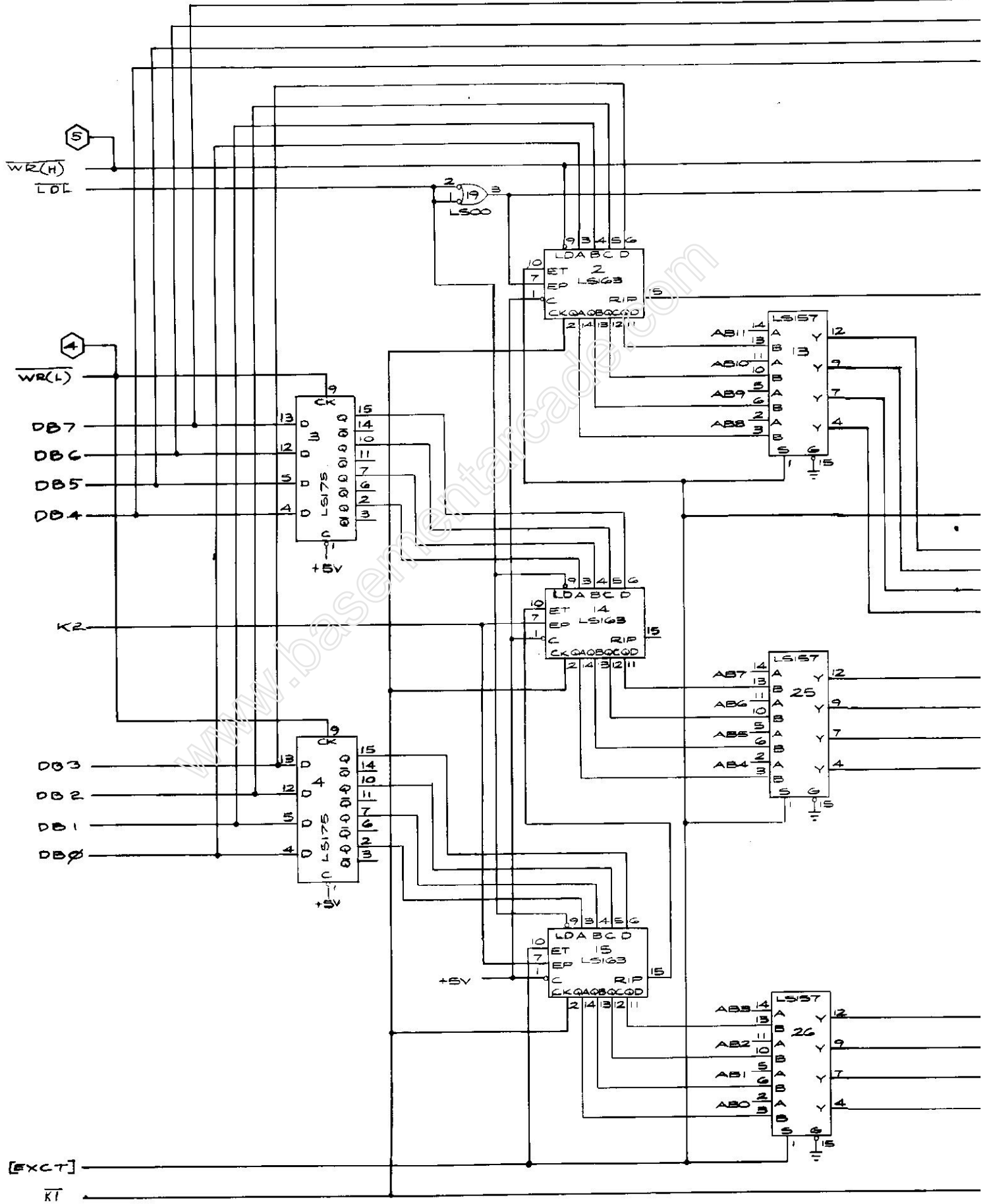
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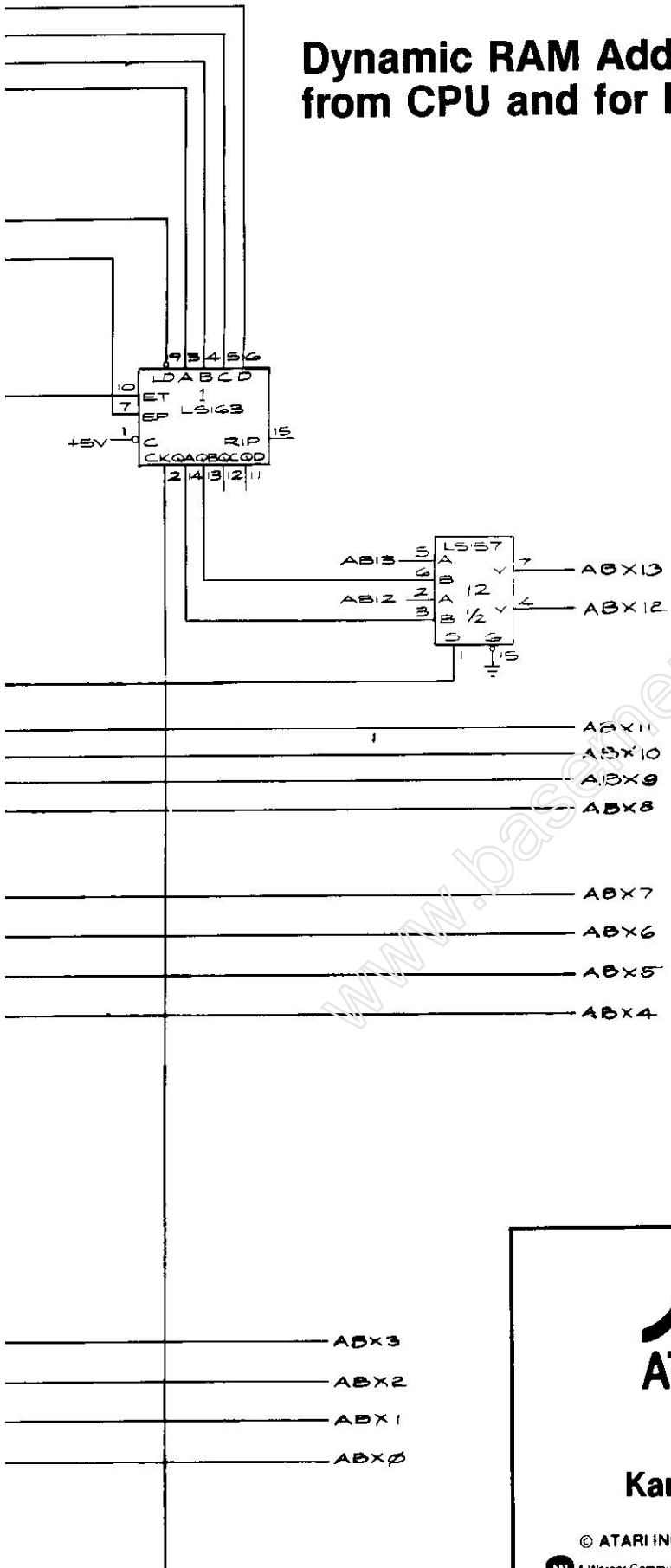
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Dynamic RAM Address from CPU and for DMA

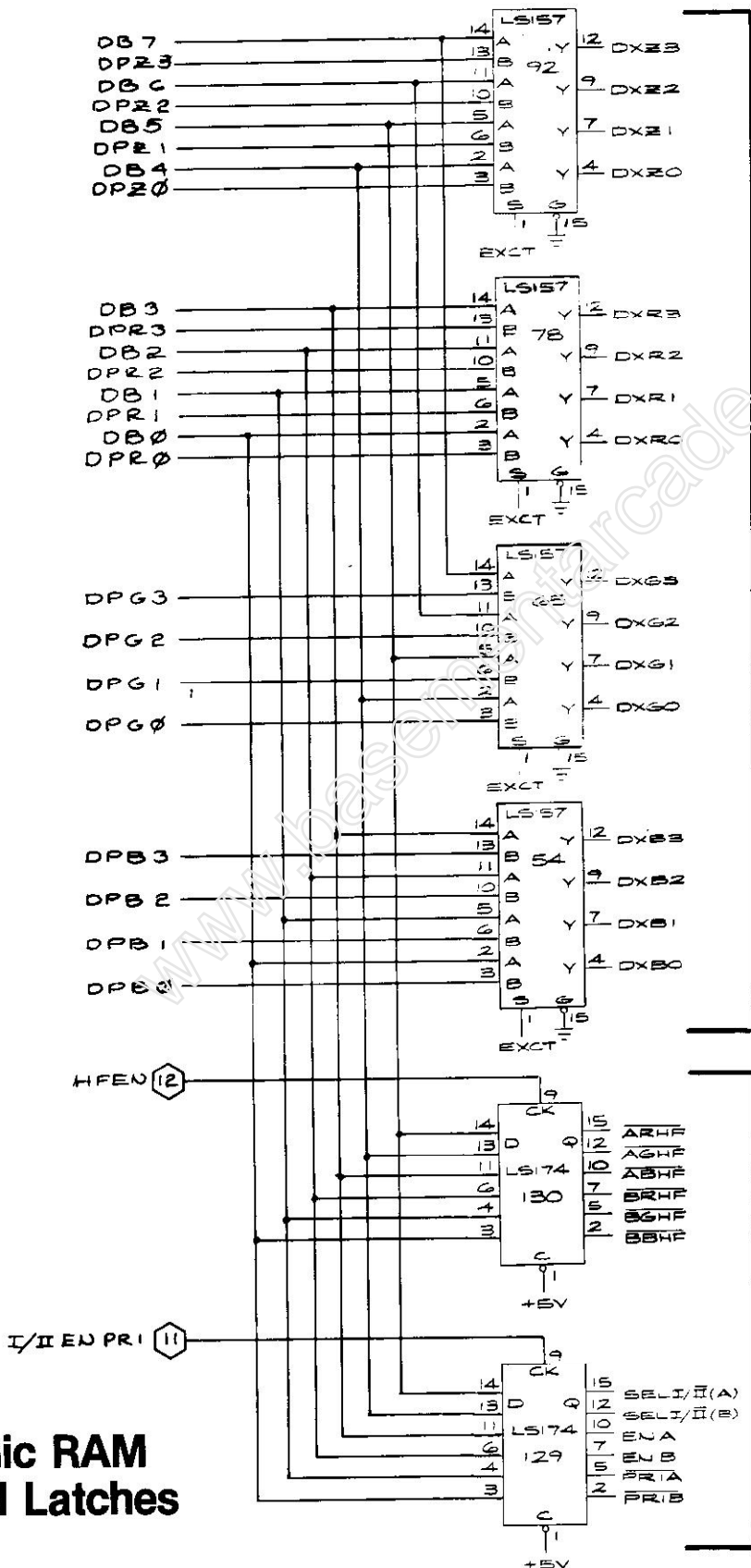


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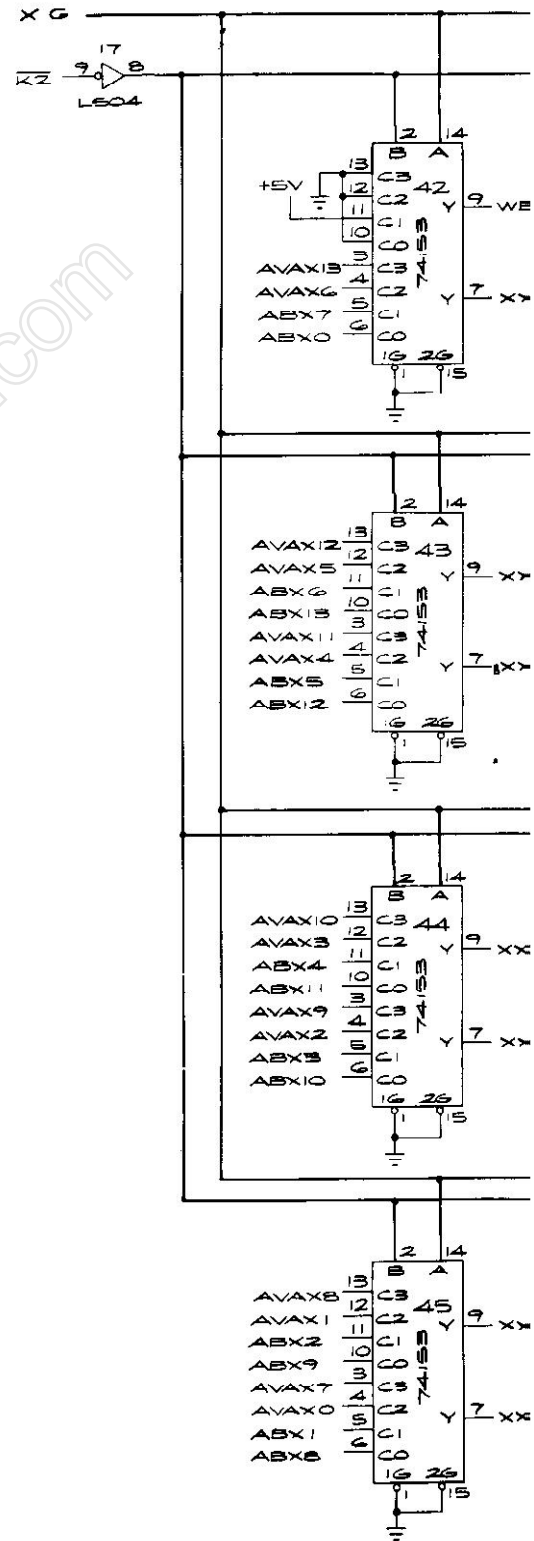
Kangaroo Video PCB Schematic Diagram

Dynamic RAM Data Selector

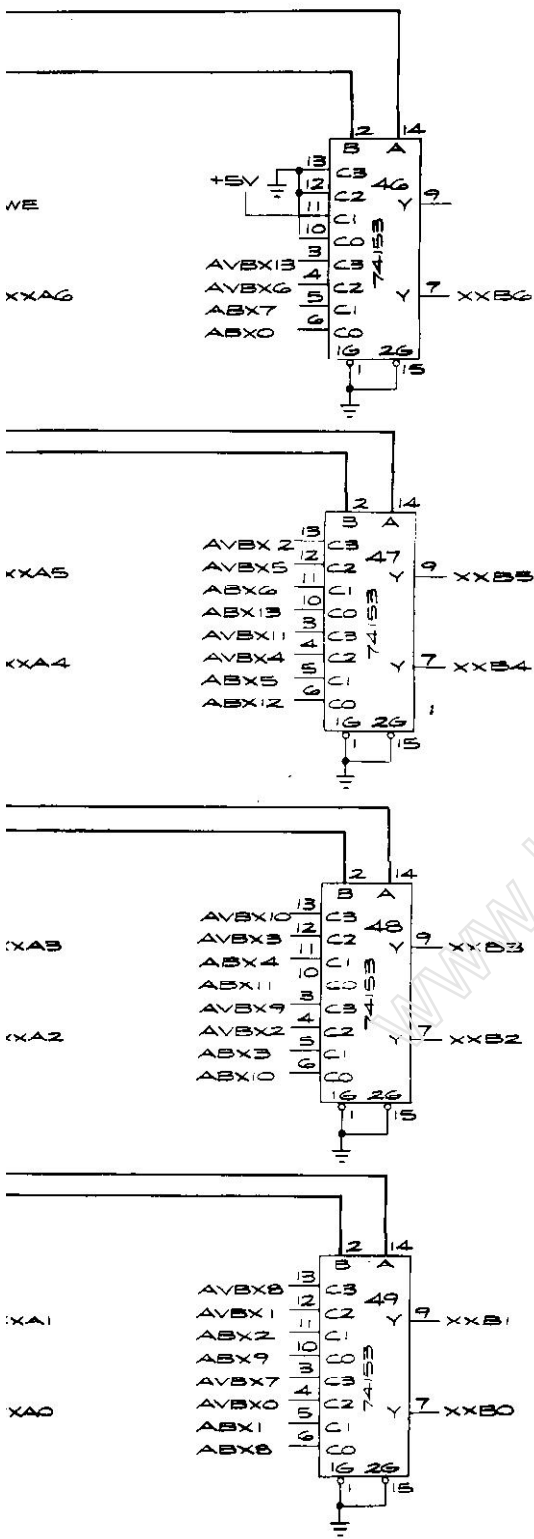
Dynamic RAM Addr



Dynamic RAM Control Latches



Address Selector



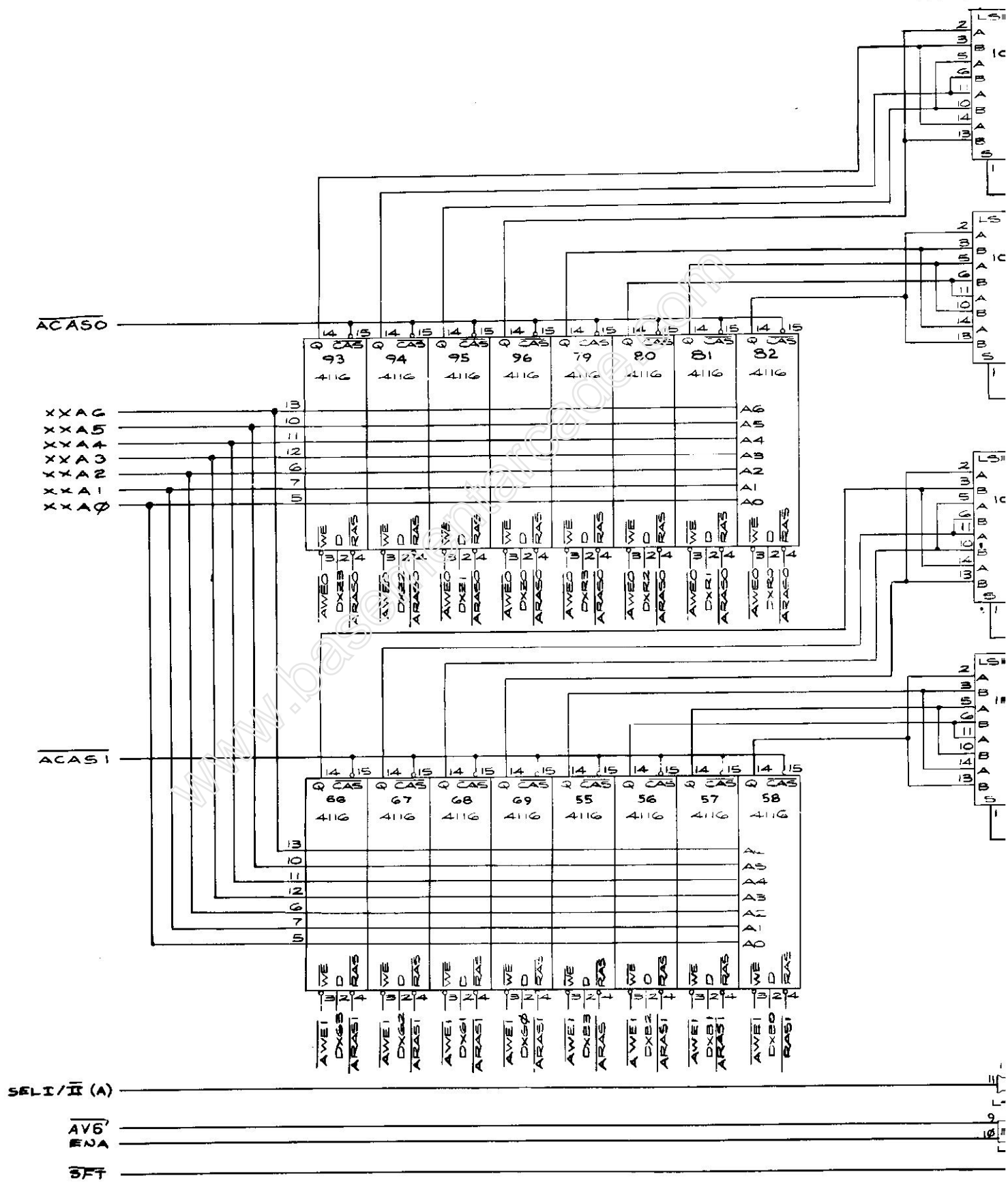
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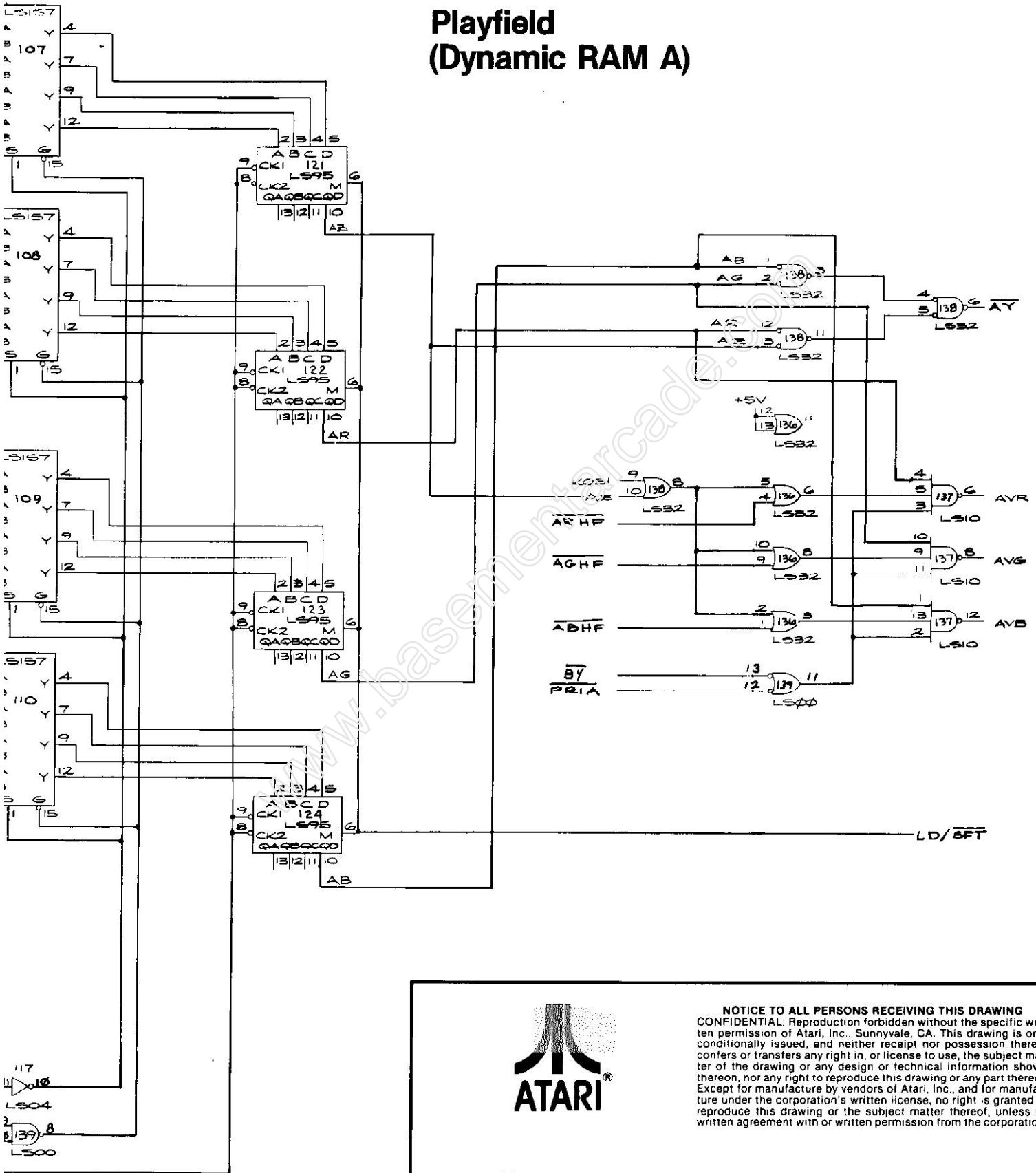
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Playfield (Dynamic RAM A)



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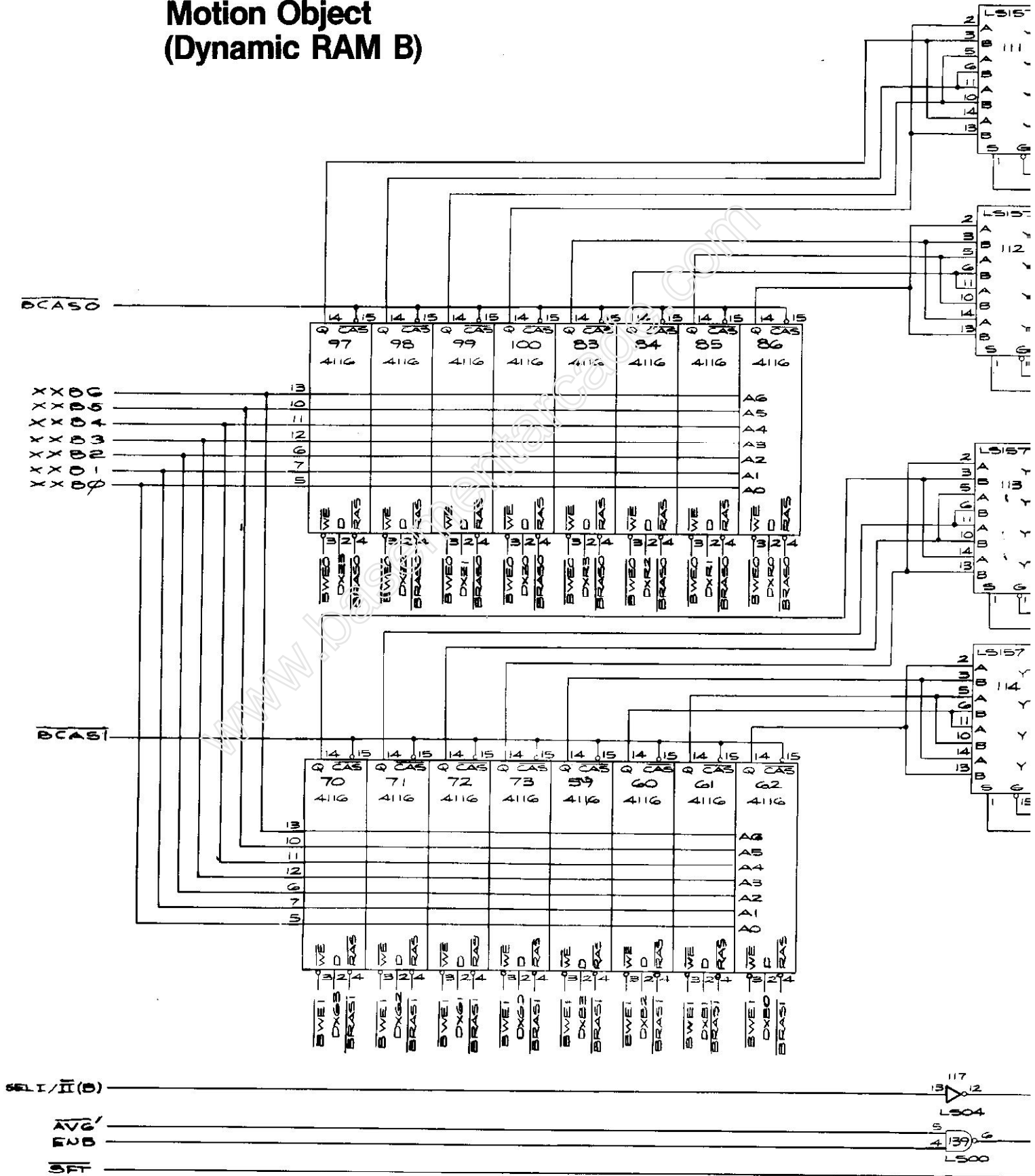
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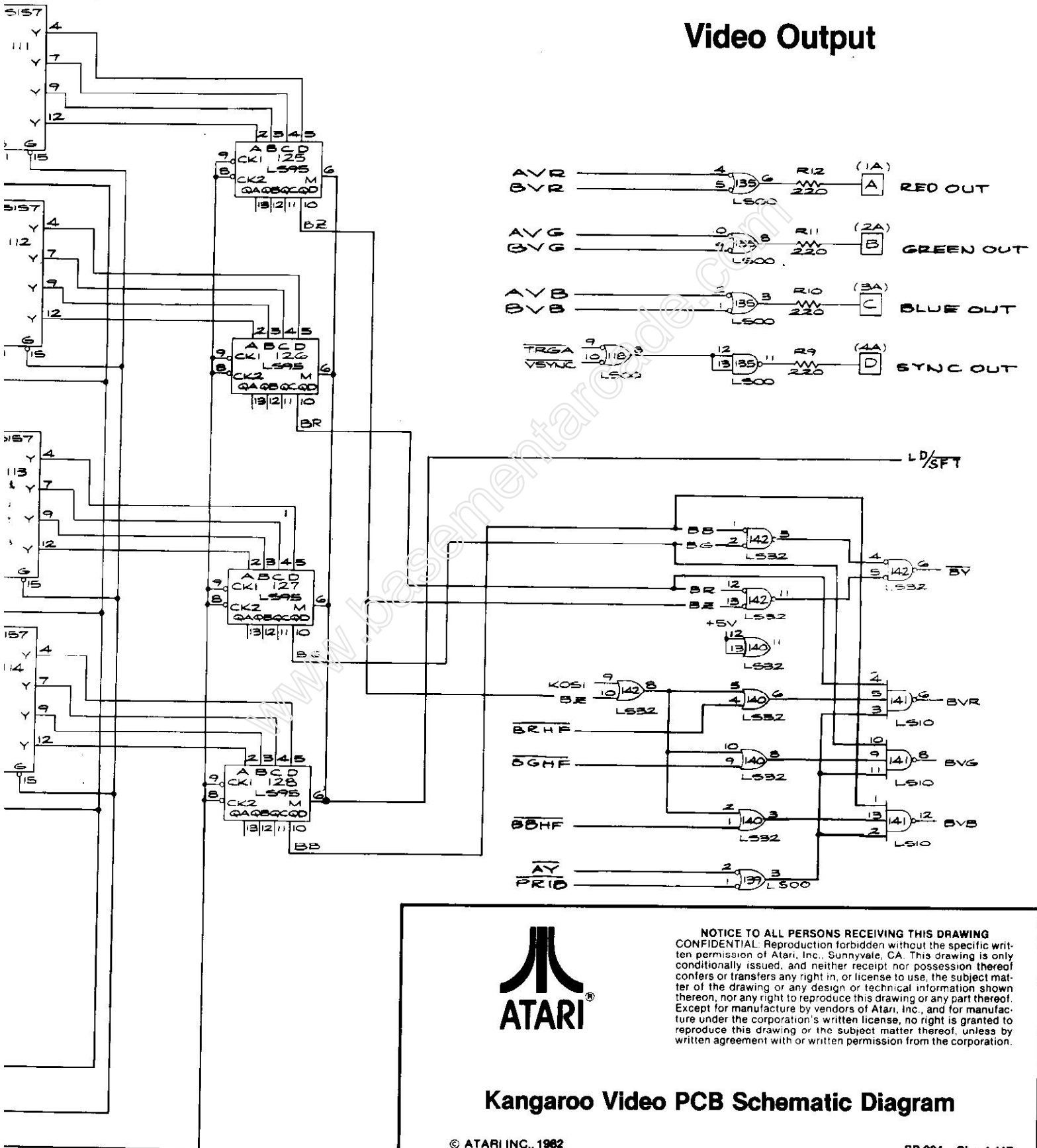
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Motion Object (Dynamic RAM B)



Video Output



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